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MEMORANDUM REPORT M70-18-1

# IDEEA PROJECT FINAL REPORT
## Part I - Network Development

by

ROBERT J. MEENAN

April 1970



**DEPARTMENT OF THE ARMY**
**FRANKFORD ARSENAL**
**Philadelphia, Pa. 19137**

## DISPOSITION INSTRUCTIONS

MEMORANDUM REPORT M70 18-1

# IDEEA PROJECT FINAL REPORT
## Part I - Network Development

by

ROBERT J. MEENAN

AMCMS Code 5910.21.20134
DA Project 2P020401A730



Fire Control Development & Engineering Division
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Philadelphia, Pa. 19137

April 1970

## ABSTRACT

This report presents the current status of the Information Data Exchange Experimental Activities (IDEEA) Network. The Network is being developed at Frankford Arsenal for the U.S. Army Information Systems Office (CRDIS-O).

A description is given of the IDEEA console equipment, internal signal flows, and the console as a systems element. Recommendations and conclusions concerning the IDEEA console and its equipment are also presented in this report.

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## GLOSSARY

| | |
|---|---|
| Alpha | Alphabetic |
| ACR | Abandon call and retry |
| ACT | Army chemical typewriter |
| ACU | Automatic call unit |
| AND | Logical Definition |
| AUTOVON | Automatic voice network (Army telephone system) |
| BA | Transmitted data |
| Baud | Bit per second |
| BB | Received data |
| C1 thru C7 | M18 computers |
| CB | Clear to send |
| CC | Data set ready |
| CD | Data terminal ready |
| CE | Ringing indicator |
| CF | Carrier detector |
| CIDS | Chemical information data system |
| CIDSII | Chemical information data system No. II |
| CRC | Cyclic redundancy check |
| CRQ | Call request |
| D-line | Output line |
| DIA | Discrete input to accumulator |
| DLO | Data line occupied |
| DPR | Digit present |
| DSS | Data set status |
| FBOO | M18 strobe line |
| GDC | Gun direction computer |
| GND | Ground |
| GPHC/ | Halt controls of the computer |
| GPRC/ | Run controls of the computer |
| I | Index register |
| I/O | Input/Output |
| IDEEA | Information data exchange experimental activities |

| | |
|---|---|
| MD | Missing data |
| Memory | A component in an electronic computing machine into which information can be inserted, stored, and automatically extracted when needed |
| MLU | Memory loading unit |
| NAND | Logical definition |
| NB1 thru NB8 | Number bit 1 through number bit 8 |
| nixie | A glow tube device which converts a combination of electrical impulses into a visual number |
| OPL | Computer-generated (discrete) lines |
| OPLE | OPL extender |
| OPLE6 | Activate feedback signal |
| P1 | Parallel Input/Output device |
| P2 | ACT |
| PB | Protect bit |
| PND | Present next digit |
| POV | Used in combination with the unprotect switch to override the protected status of a record and enable writing |
| PV | Protect violation |
| R | Ready bit |
| RGO | Output signal which goes true when FADAC is in an "input external device" condition |
| RHO | Inverse of RGO |
| RP | Bit which must be set in order to change the protect/unprotect indicator for a record |
| SA | Sector available |
| S1 thru S3 | Data phone or serial I/O device |
| T1, T2 | Bulk storage units |
| TEIP | Output from GDC M18, used in conjunction with information input (inverse of the TG signal) |
| TFBO | Feed back line |
| TG | Strobe term |
| WD | Write disable |

# INTRODUCTION

The IDEEA (Information Data Exchange Experimental Activities) Network is an exploratory development project conducted by Frankford Arsenal for the U.S. Army Information Systems Office (formerly Army Research Office) in Washington, D.C. The purpose of the network is to collect data on the various aspects of the man-machine interface of computerized information storage and retrieval systems. By providing scientific and engineering personnel with the means for gaining access to automated technical information files, study data can be obtained as the system is used. The data obtained from these experiments could be used to determine the best means and methods of information retrieval. The IDEEA network was designed to collect usage information necessary for efficient system design in order to provide the government with the best available information system at minimum cost.

The IDEEA network is composed of interconnected individual self-sufficient stations. The stations were constructed from available hardware to facilitate their completion and to provide an operational system at minimum cost.

Originally, a five-station network was planned. The network was set up with a chemical information retrieval capability since it was planned that each station be located at a U.S. Army installation which has a specific chemistry interst. To date, three stations have been completed and are working. Each network station can be connected to either the Autovon (Automatic Voice Network) or commercial telephone systems so that information may be interchanged between stations in the network.

IDEEA is not limited to handling chemical information, but efforts were concentrated on a chemical information retrieval system for the proposed study because:

1. Chemical information systems were felt to be the most organized of technical data systems.

2. A companion project, CIDS (Chemical Information Data System), was under development by the University of Pennsylvania for Edgewood Arsenal and was expected to provide a data bank for use in the experiment.

3. The Army Chemical Typewriter (ACT), developed for Walter Reed Army Institute for Research, provided an available input-output device.

Each station of the network (Figure 1) contains a small general purpose computer, communications facilities, a chemical typewriter for input-output, a disc type bulk storage unit, and a digital clock.

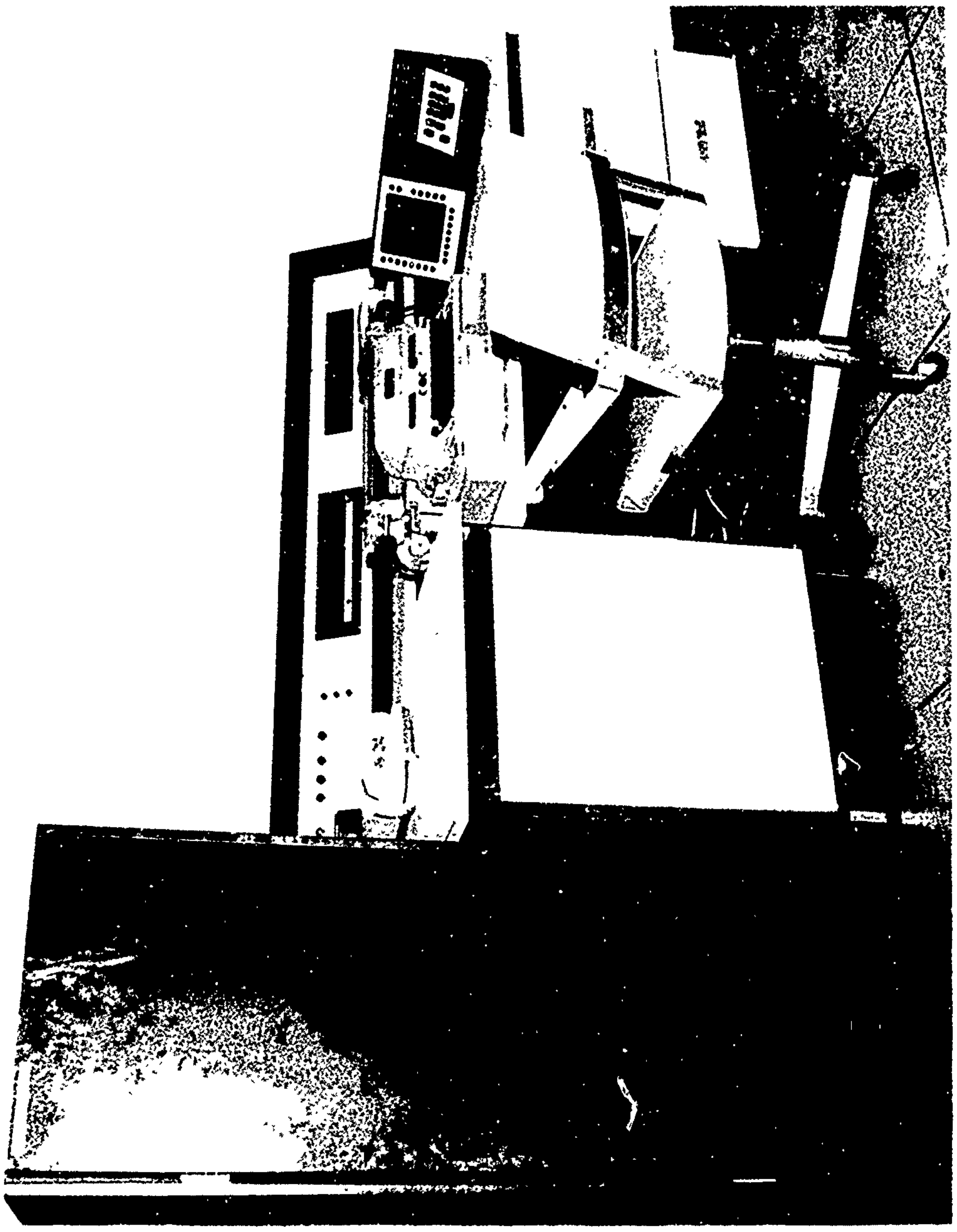


Figure 1. IDEEA Network Station

With this equipment a station can store, receive and send data, and log each query, as well as provide hard copy and/or paper tape representations of processed information.

## IDEEA NETWORK CONCEPT

The originally planned five-station IDEEA network is illustrated in Figure 2. The network is composed of individual stations, each with the capability to store, receive, send, and provide a hard copy and/or paper tape representation of chemical information. The IDEEA network has the capability of interconnecting a number of different pieces of digital equipment. Any piece of equipment that is data-phone interfacable can exchange data with the IDEEA stations. Examples of equipment that can be interconnected are teletypewriters, cathode ray tube displays, commercial computers, etc.

The IDEEA network was developed by integrating available hardware into a functional system. The advantage of this approach was that the network could be implemented with a minimum amount of equipment development. The major disadvantage was that none of the available pieces of equipment were specifically designed for an information exchange network. A basic objective of the IDEEA network implementation was to provide a functional network as quickly as possible so that actual experience and use data could be obtained to guide the specification of hardware for future data exchange systems.

Each IDEEA Station was designed to have its own bulk storage device to store data and programs, the means of inputting and retrieving data from storage, a means of logging usage information, an Automatic Call Unit (ACU) for automatic placement of telephone calls, telephone data sets to receive and transmit digital data, and a small digital computer to provide control and digital processing capabilities. By using the Autovon or commercial telephone system, any IDEEA station located at any Department of Defense installation has the means of interchanging data with any data bank that can be connected to telephone lines. The IDEEA console has been used to simulate a teletype in querying the CIDSII data bank presently located at the University of Pennsylvania. The University of Pennsylvania uses a small scale commercial computer as a controller for and communications buffer to their large scale computer.

## IDEEA STATION EQUIPMENT

The IDEEA Station equipment is a combination of commercially available pieces of equipment and of equipment available through the military supply system. The digital clock, disc memory unit, and

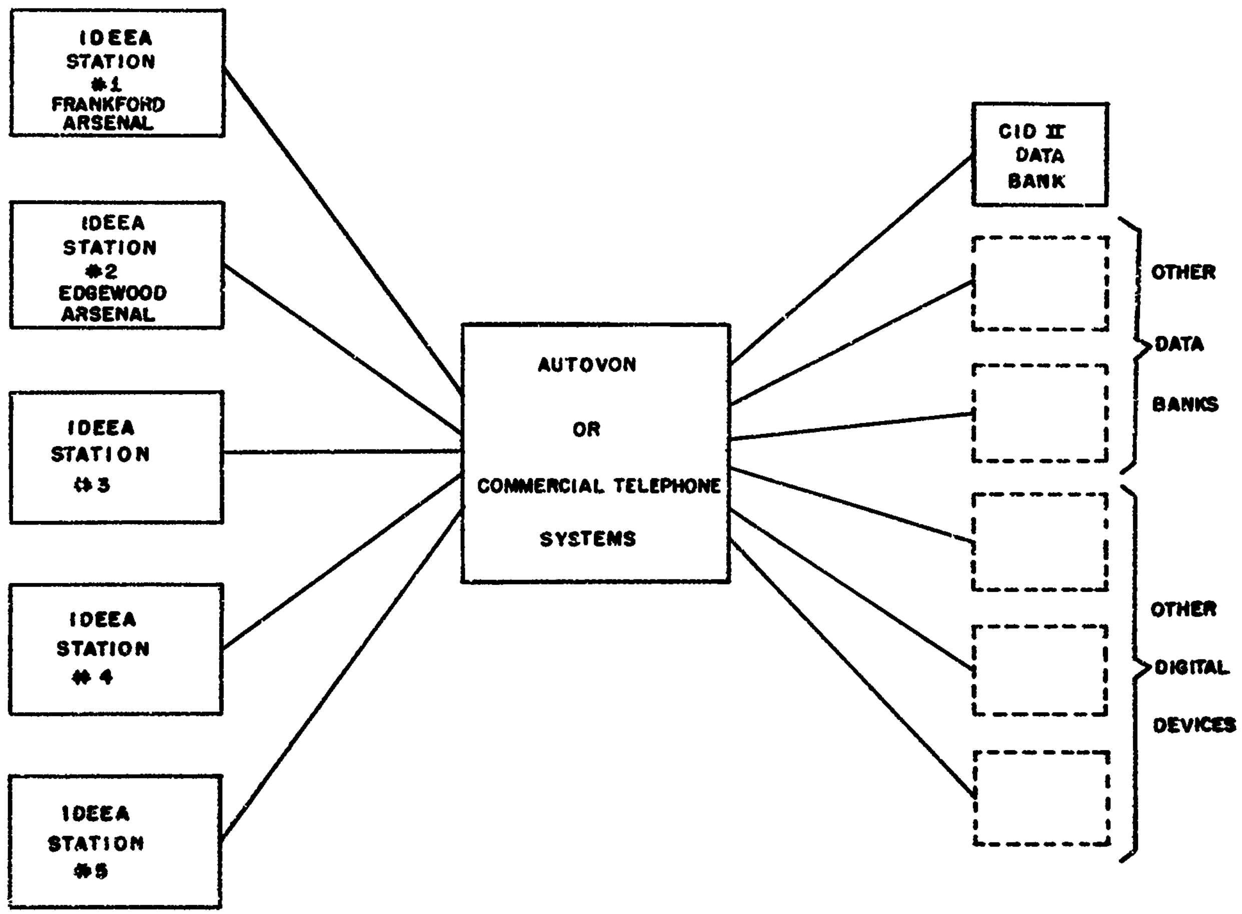



Figure 2. IDEEA Network

controller unit are purchased commercially, the digital clock and the controller for the disc memory units being modified, off-the-shelf, commercially available items, while the disc unit itself is used as-received and requires no modification. The pieces of equipment obtained within the military supply system are the Gun Direction Computer, M18, and its peripherals. The Army Chemical Typewriter was obtained from the Walter Reed Army Institute for Research. These items are described in the following paragraphs.

## M18 Computer

The Gun Direction Computer, M18, is a second generation, solid state, general purpose, digital computer. The M18 was developed by Frankford Arsenal for field use in solving ballistic problems to obtain first round effective fire. As used in the IDEEA station, the M18 provides the automatic control and computational capabilities which permit each station to be operated by personnel with no training in chemistry, electronics, or computer programming.

As received in its field case, the M18 computer (Figure 3) was modified to facilitate mounting it in the IDEEA console. The control panel of the M18 was removed from the main frame. The "nixie" display package was removed and mounted on the front panel of the console. The keyboard, matrix, indicator lights, and control buttons were repackaged and mounted on the right hand side of the console shelf, permitting the operator easy access to the keyboard and control buttons.

The main frame of the M18 was removed from its field case and opened. This section contains the magnetic memory assembly, power supply assemblies, and computer electronics. It is mounted in the console on chassis slides, allowing it to slide out for easy access. To facilitate maintenance procedures, the M18 is free to rotate a full 90 degrees in either direction from its upright position (Figure 4). This rotation permits ready access to both printed circuit cards and connector wiring.

As shown in Figure 5, the Control Unit of the M18 processes and interprets all machine functions and also controls internal and external information flow via the input-output lines.* An instruction is read from "memory" and routed to the I register. There it is analyzed and the operand read from memory. The control unit then instructs the arithmetic unit to perform the operation.

*Gun Direction Computer XM18 (FADAC) - Programming Manual," Frankford Arsenal Notes on Development Type Materiel," FCDD-361, Volume IV, Rev 1, November 1962.

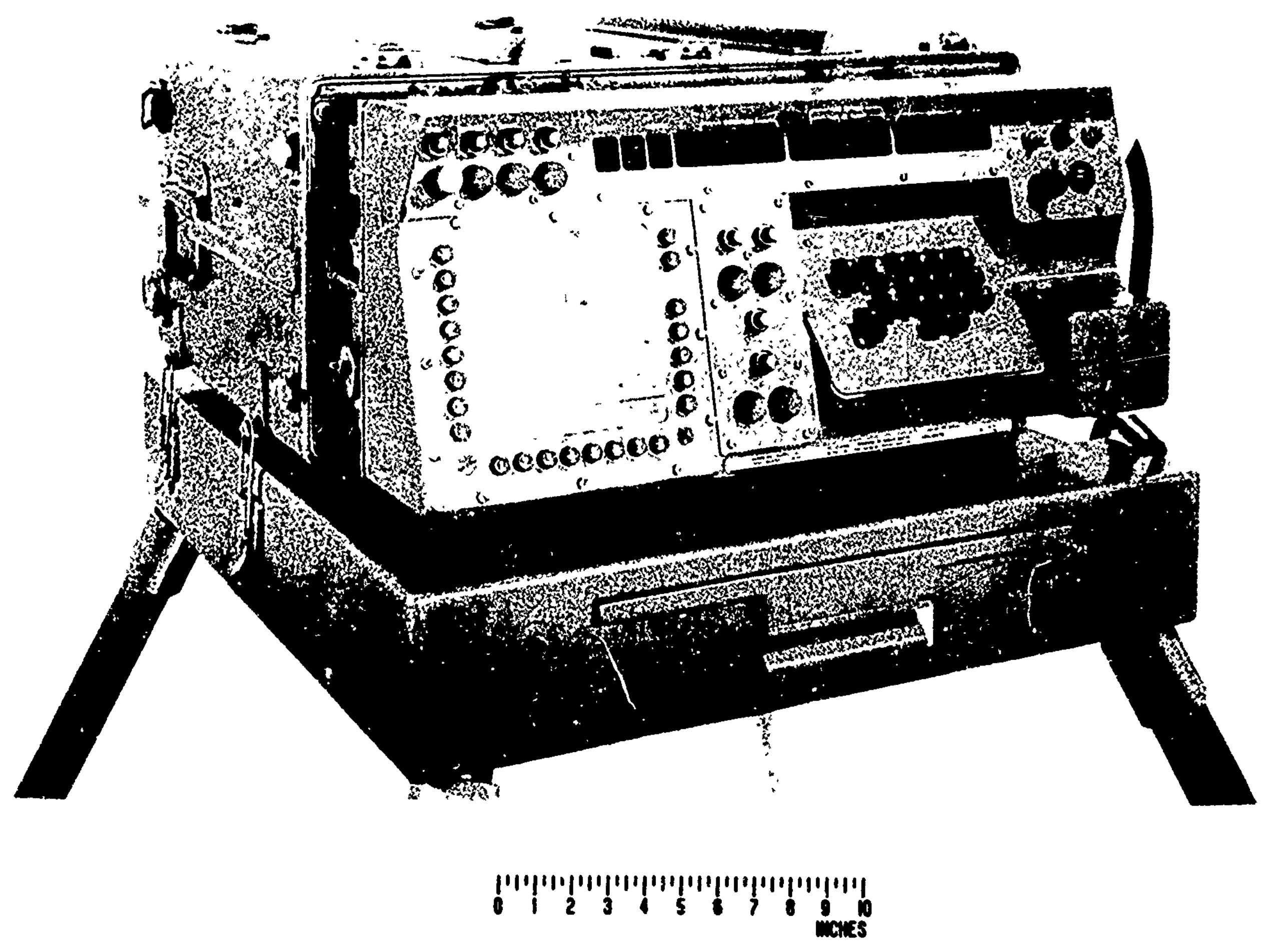



Figure 3. M18 Computer in Field Case

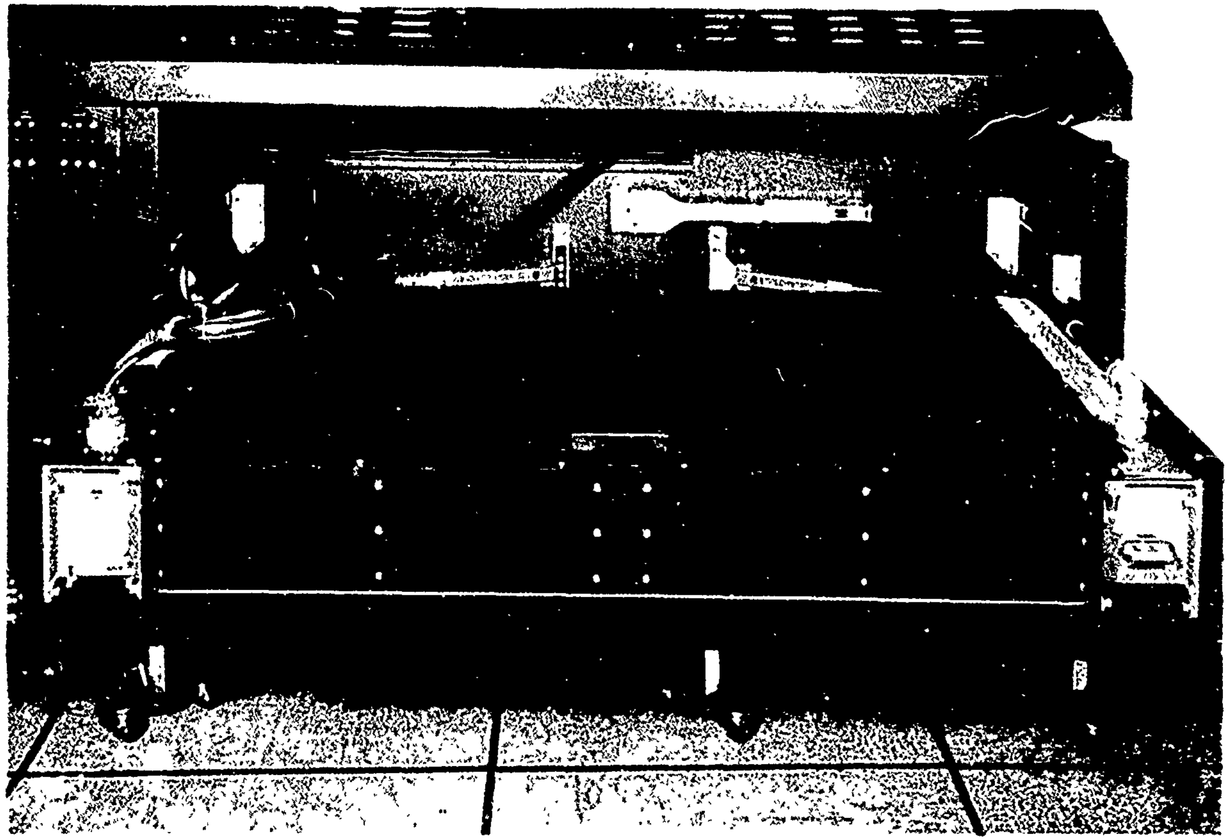


Figure 4. M18 Computer in IDEEA Console

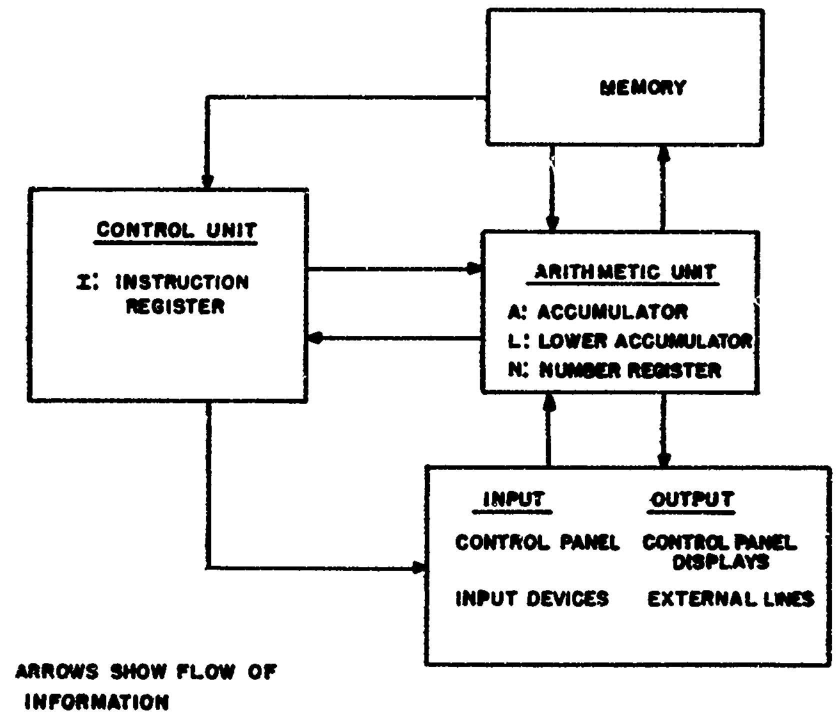



Figure 5. Functional Diagram of the M18 Computer System

Three registers make up the arithmetic unit: the accumulator (primary register), lower accumulator, and number register. The accumulator is used as one of the input-output buffers and is also used in all arithmetic, logical, and decision operations. In some operations the lower accumulator is used as an extension of the accumulator while in other functions the lower accumulator acts independent of the accumulator and serves as part of the control for input-output functions. For some operations, the number register holds the second operand. This register is employed as one of the input-output buffers and also serves in program control transfer operations.

The internal memory of the M18 computer is a rotating magnetic disc coated with ferrous oxide, similar to the coating of magnetic tape. The disc rotates under stationary read and write heads at approximately 6000 rpm. Memory capacity is 8192 words, each word consisting of 32 information bits.

Since the computer is in the military supply system, the peripheral equipment, spare parts, operational manuals, etc., as well as trained maintenance and programming personnel, are available. A Signal Data Reproducer, AN/GSQ (memory loading unit), is provided with each IDEEA station. This device is a militarized paper tape reader (600 characters per second) and is used to load the M18 computer memory.

## Army Chemical Typewriter

The Army Chemical Typewriter (ACT) (Figure 6) is the primary input/output device of the IDEEA console. It is a modified, commercially available, electric typewriter developed for the Walter Reed Army Institute for Research as a means for preparing chemical structure diagrams for storage in a computer for subsequent searching and retrieval. Modifications to the commercial typewriter included the addition of a third case for symbols used to create chemical structures and, also, a coordinate generation system, permitting the operator to type a structure in any convenient order and, also, to return to any desired portion of the structure for error correction.

The upper and lower cases are almost identical to the standard upper and lower cases of all electric typewriters. These cases provide standard upper and lower case alphabetic (alpha), numeric, and punctuation characters. The third case provides the special characters required for the generation of structure diagrams (Figure 7). The ACT will accept data either by insertion of punched paper tape or by manual operation of the keyboard.

When preparing a chemical structure by using the keyboard, the operator types the required characters and manipulates the platen to obtain a hard copy of the desired structure having the correct

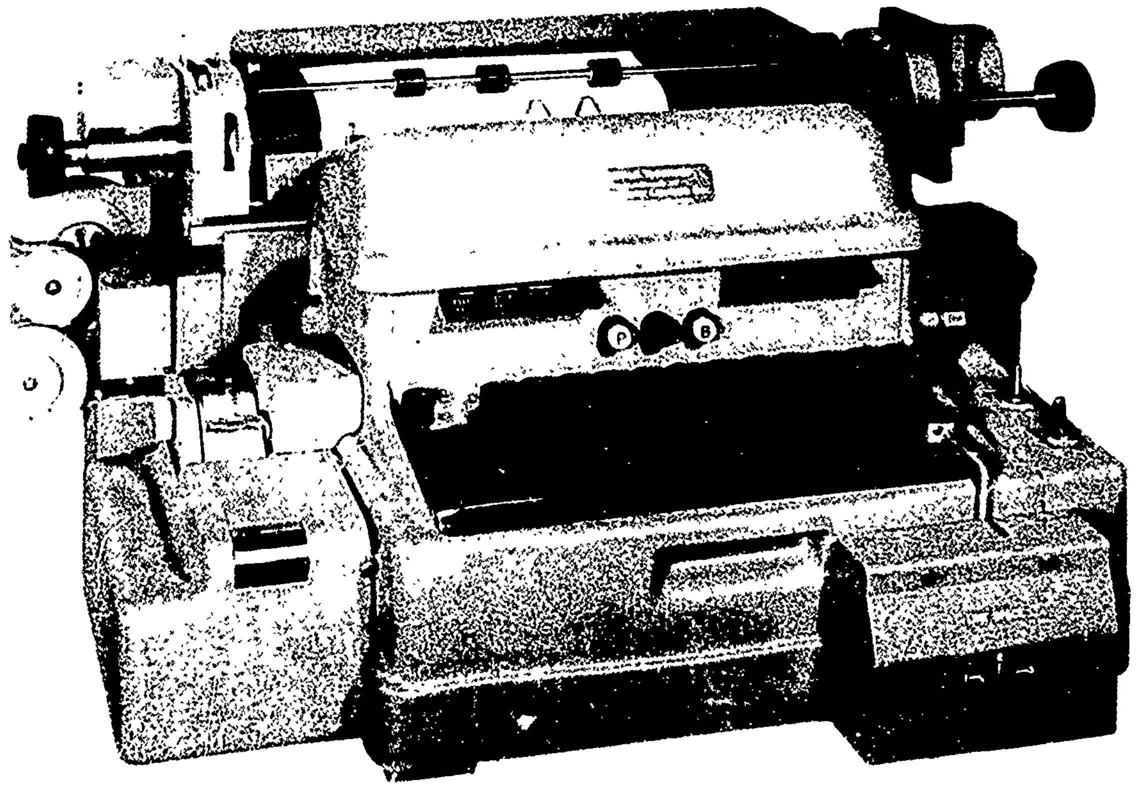
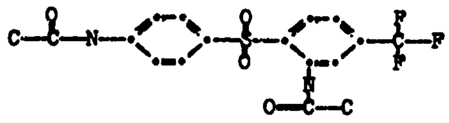


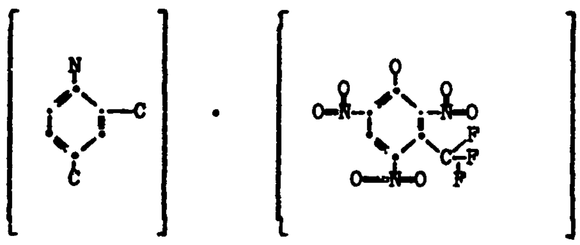
**Figure 6. Army Chemical Typewriter**

◇
RN 384443 (CAS) $C_{17}H_{15}F_3N_2O_4S$



STEREO N
**

◇
RN 384758 (CAS) $C_{15}H_{13}F_3N_4O_7$



STEREO N
**

Figure 7. Structure Diagram

configuration. In preparing a structure diagram in this manner, a paper tape is punched with both structure and coördinate information. Coordinate information is only generated for the first character after a positioning function (such as back space, tab, line advance, carriage return) or whenever the platen is manually positioned. This allows the operator, by the use of function keys or platen manipulation, to type structure diagrams in the most convenient order and also permits returning to any position on the page for correction.

A paper tape (coordinate tape) generated during this procedure cannot be run through the mechanical reader for a hard copy representation of the typed structure. Instead, the data of a coordinate tape must be rearranged and a line-by-line output tape made. To produce a hard copy by paper tape, data must be supplied line-by-line since the ACT has no reverse line feed capability.

The ACT is, in itself, a multiple piece system made up of the typewriter and attached tape reader, a power supply chassis, a logic card rack, and an associated paper tape punch. The typewriter with its paper tape reader is placed on the console shelf such that it is readily available to the operator and has no obstructions to inhibit its operation (Figure 8). The ACT power supply chasis, which provides the required voltages to the typewriter and logic cards, is mounted in the upper portion of the left hand compartment of the console.

The ACT logic card rack is combined with the required IDEEA interface electronics to make up the IDEEA interface chassis (Figure 9) and is mounted in the lower portion of the left hand compartment. The paper tape punch is placed in the top drawer on the right hand side of the console, thus giving the operator easy access to punched tapes. The interconnecting cables for the ACT were left intact and routed through the console.

Using the ACT presented many problems because it was not designed as a systems device. It had to be modified to permit operation in the system. A connector was mounted on the rear plate of the typewriter to permit access to typewriter sense lines. Data output lines from the punch and reader coils were brought out. The ACT mode select switch was rewired to permit automatic output from the reader coils whenever the tape reader is to be used. In normal operation all output signals are taken off the punch coils but, by using the reader, much faster operation is achieved.

Inputs to the typewriter from the translator were also brought out. Through the use of the interface electronics, inputs to the typewriter may be made through the translator, producing a hard copy, or may go directly to the punch to produce a paper tape representation.

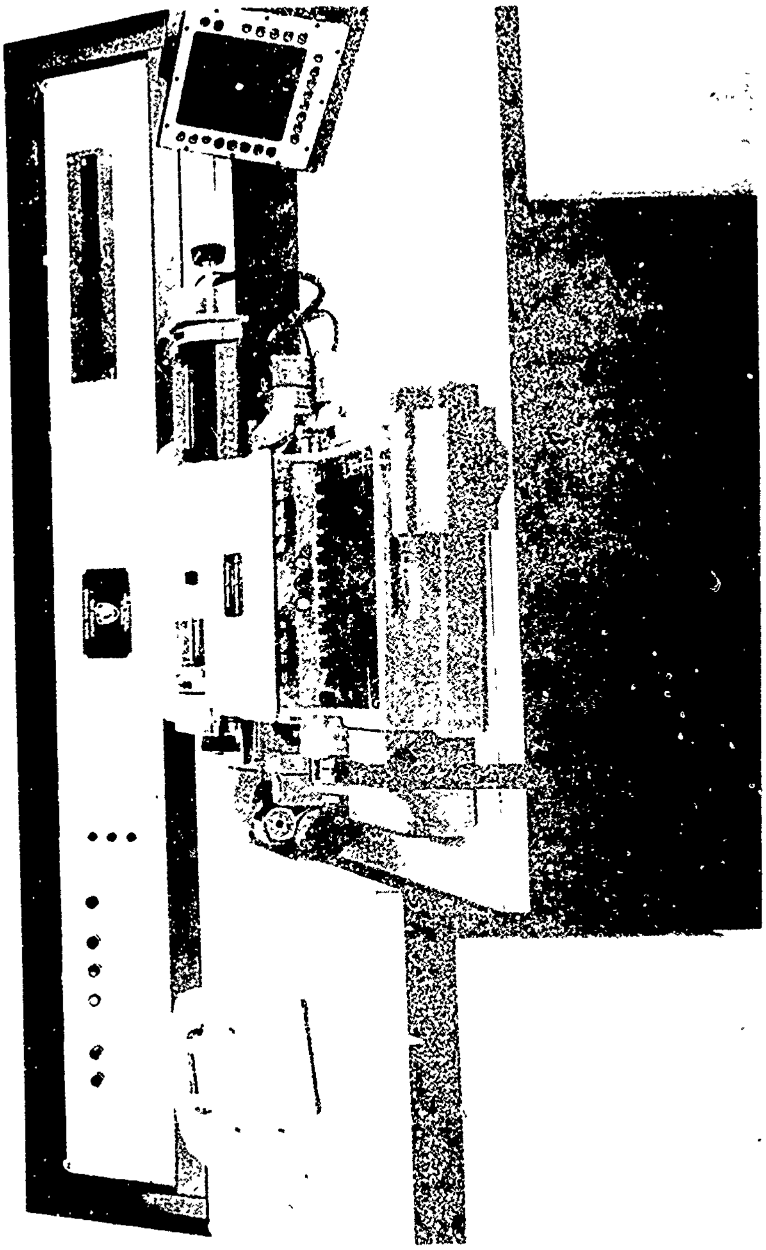


Figure 8. Army Chemical Typewriter (ACT) on IDEEA Console

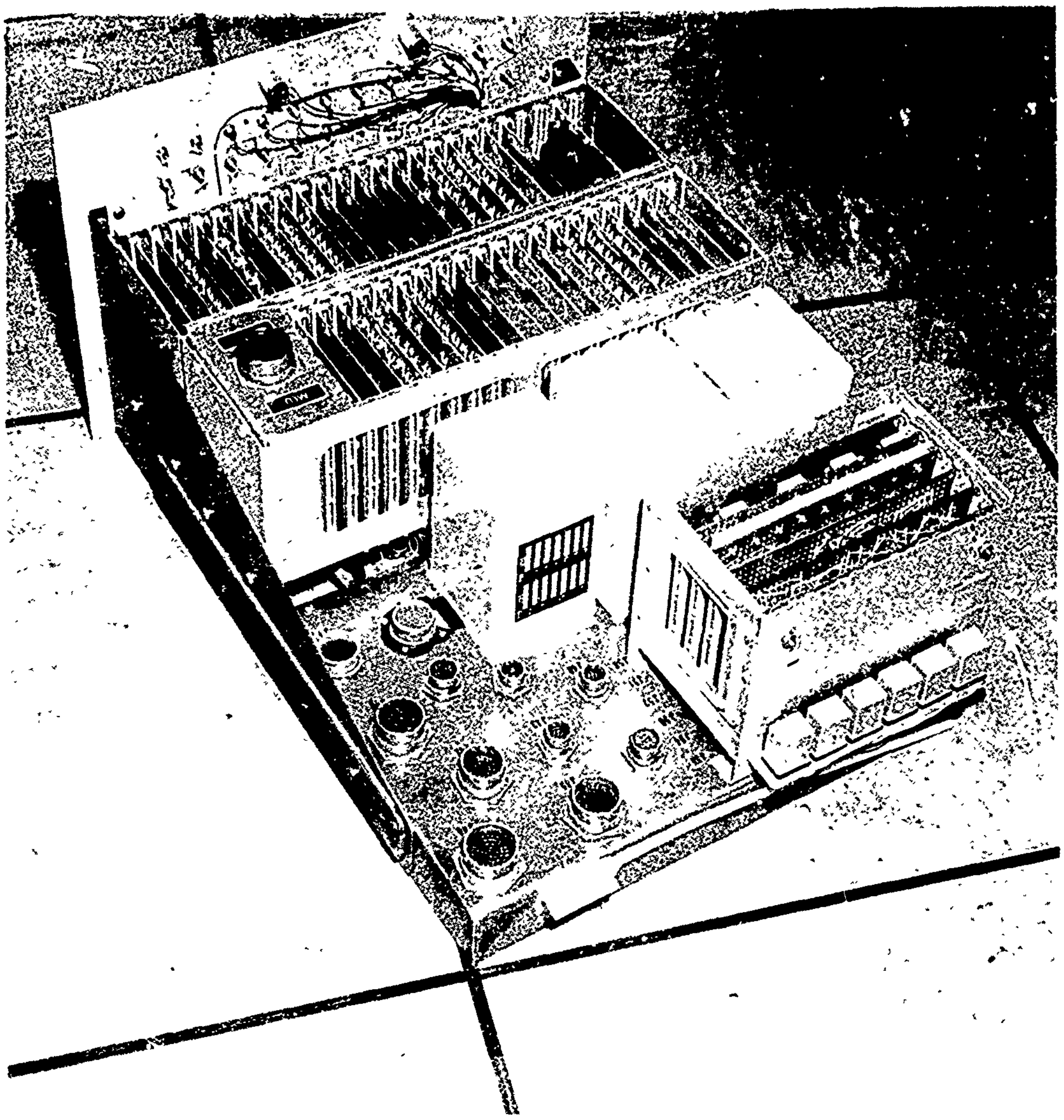


Figure 9. IDEEA Interface Chassis

A parity off-switch was added to the typewriter; this removes the parity check from the punch and permits any coding scheme to be punched out on the ACT punch. Additional lines and internal changes in the ACT were made in order to obtain timing and feedback signals. A line was added to inhibit input to the typewriter during mechanical functions (such as line advance, carriage return, case shifts, etc.) which require longer periods of time than typing standard characters. Control lines were also added to automatically start and stop the reader, lock the keyboard, switch modes, and provide for punch output. In addition, a new line advance mechanism (Figure 10) was designed and mounted on all network machines. This change permits direct actuation, achieving much more reliable operation.

## IDEEA Digital Clock

The IDEEA Digital Clock (Figure 11) is used to log usage information such as length of query, length of answer, total time to complete data exchange, etc. It is an all solid-state instrument, using integrated circuits and silicon semiconductors.

The clock uses modular construction, with all active circuits on plug-in printed circuit cards. Timing is obtained from the 60 Hz power line by means of a synchronized flywheel oscillator. This provides timing pulses that are not susceptible to power line transients. The clock is equipped with a power line failure circuit. When AC power drops below the preset level for more than three cycles, the circuit trips and resets the clock to all zeros.

The clock displays time of year in days, hours, minutes, and seconds. The display uses nine nixie indicators. There is a 10-position rotary switch for setting the time, a push button for starting, and a toggle switch for 365 or 366 days. Two output connectors are mounted on the side panel of the clock.

## Bulk Storage Unit

The Bulk Storage Unit is composed of a Disc Memory Unit and a Controller. The disc memory unit is commercially available. It is a random track access memory module for interface with digital computers and/or other digital devices. It accepts a serial digital input, records it by saturation magnetic recording at up to 3300 bits per inch, and delivers a clocked serial digital output of the memory content on command.

The disc electronic system contains a single read amplifier for the data heads. Data is written onto and read from only one data track

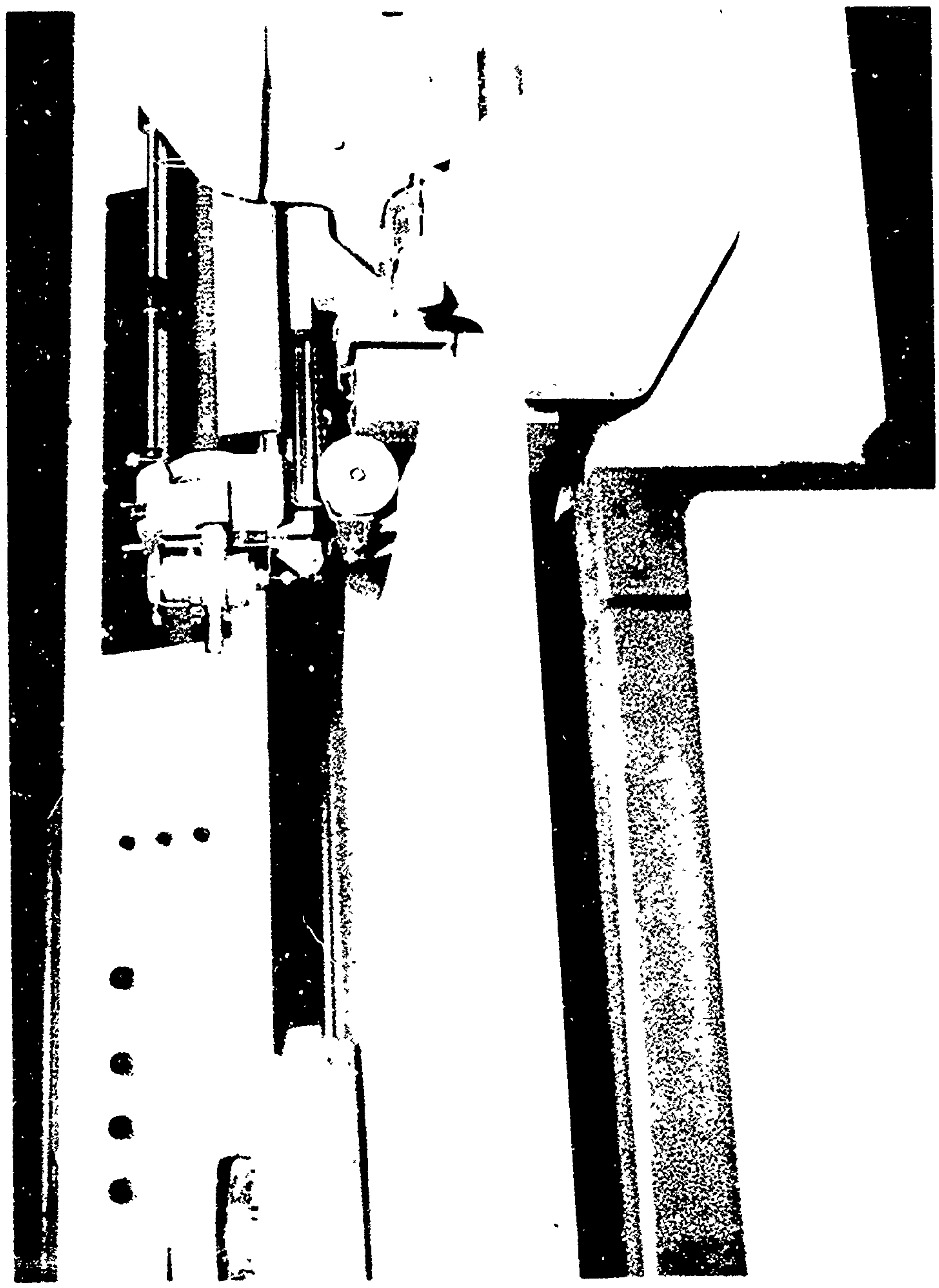


Figure 10. Line Advance Mechanism

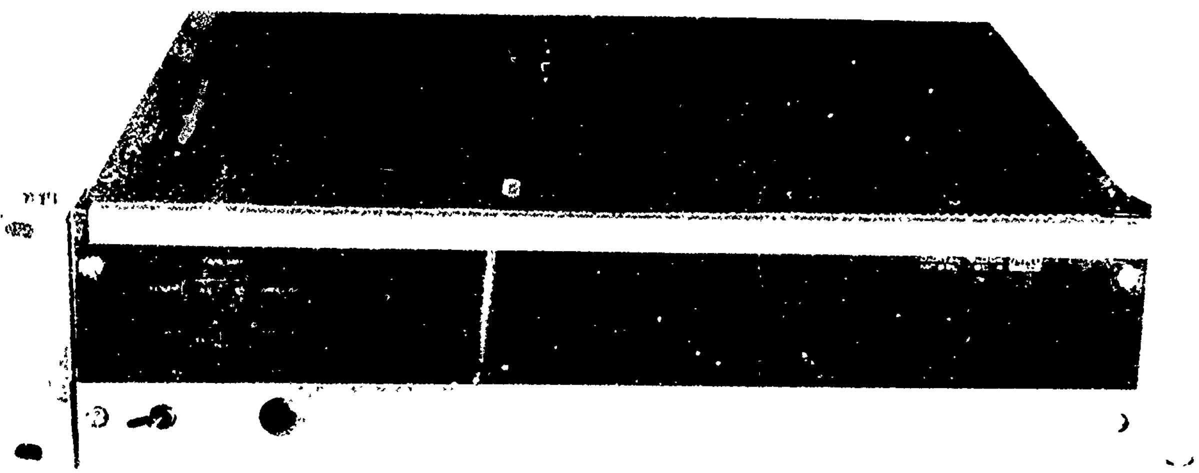


Figure 11. IDEEA Digital Clock

at a time. An electronic head-switching matrix provides interconnection between the read and write amplifiers and any one of the data heads. The data heads are arranged electrically into a two-dimensional selection matrix where a particular head may be selected by defining the two coordinates of the head.

The physical characteristics of the disc pack when utilized with the M18 computer are:

(1) Track size: 64
(2) Sectors per track: 128
(3) 32 bit words per sector: 16
(4) Word capacity: 131,072 per disc
(5) Average access time: 16.7 milliseconds.

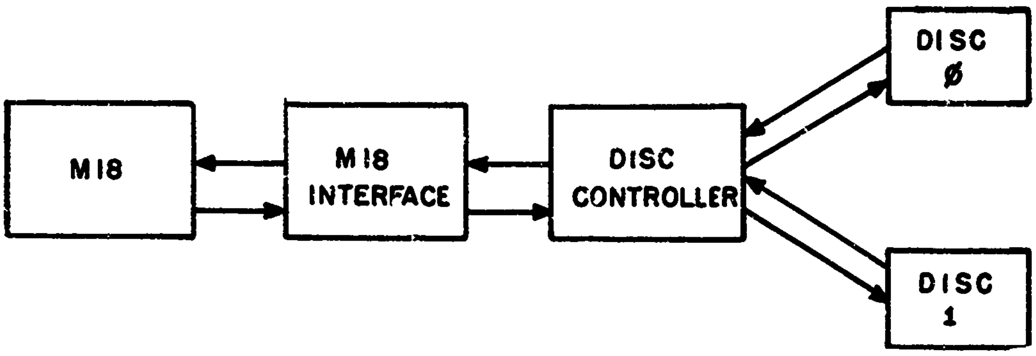



Figure 12. M18 Computer-Disc Pack System

As illustrated in Figure 12, the IDEEA Bulk Storage Unit contains a disc pack, a disc controller, and disc pack-to-M18 computer interface circuitry. These units are packaged together in a cabinet, which is called the IDEEA Console. There is space in the cabinet to house a second disc pack, together with the required additional wired card slots and sufficient power supply capacity. Thus, the capability of the bulk storage unit could be doubled by adding another disc pack and circuit cards to the present cabinet. The controller could also handle two more disc packs external to the present cabinet. Figure 13 shows the IDEEA Bulk Storage Unit.

## 103A2 Data Sets

There are two 103A2 data sets (for communication lines) contained in the IDEEA console. These data sets are mounted in the lower drawer, on the right hand side of the console. They provide for the transmission of binary serial data in data phone and TWX services. In data phone service, the sets permit transmission rates up to 2000 bauds (200 bits/second) maximum, in either or both directions. Through the use of two data sets, the IDEEA station has store and forward capabilities.

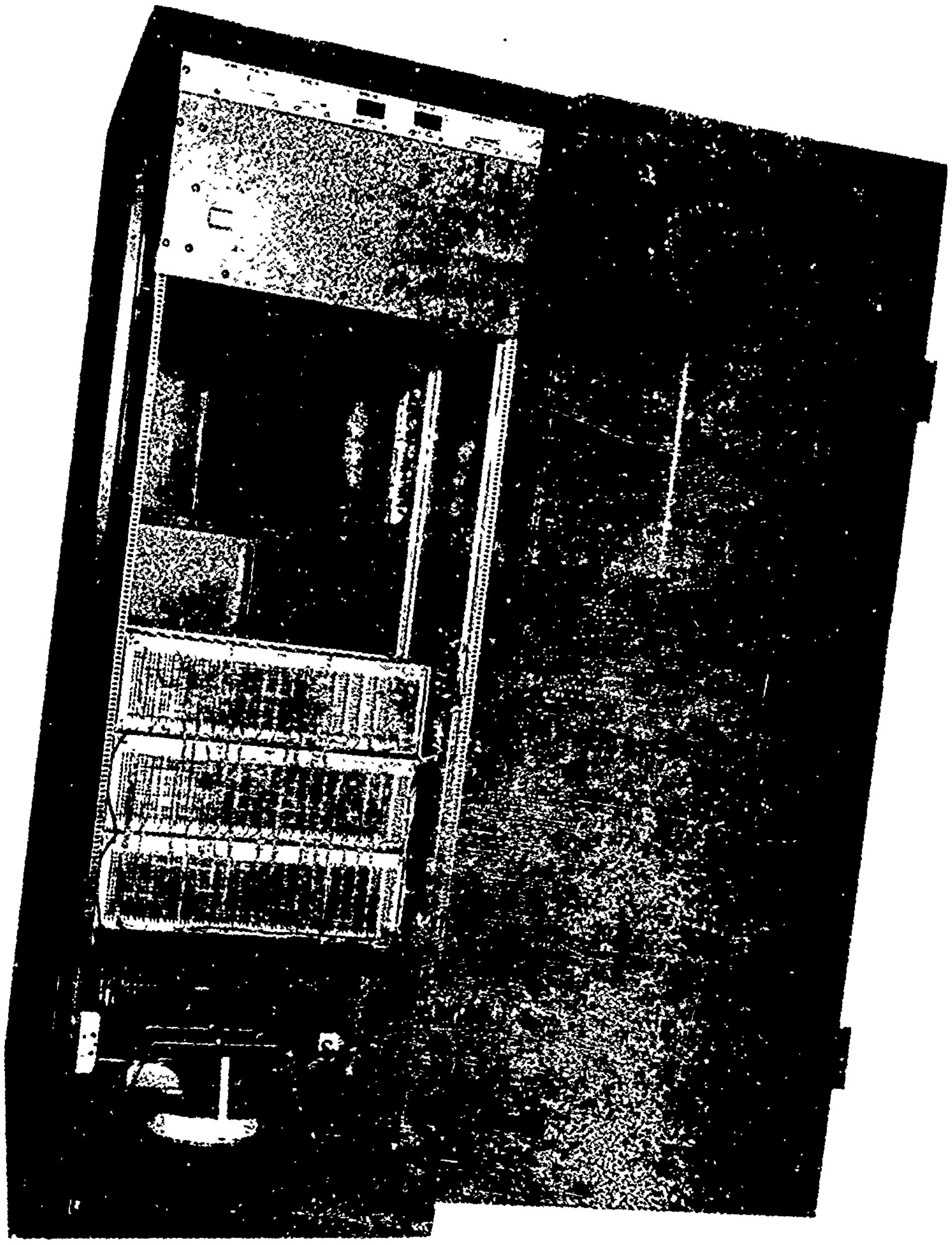


Figure 13. Bulk Storage Unit

### Automatic Call Unit

The Data Auxiliary Set 801A3, the automatic calling unit (ACU) in the IDEEA station, permits the computer to originate data phone calls automatically. Instructions and the number to be dialed are passed between the computer and the automatic call unit in the form of binary electrical signals. Digits to be dialed are presented to the automatic call unit, one at a time, in four-lead binary form. As each digit of the telephone number is dialed, the automatic call unit requests the next digit from the computer, until dialing has been completed.

## DATA AND SIGNAL FLOW ANALYSIS

### IDEEA Interface

Figure 14 presents a simple signal flow block diagram of the IDEEA station. All signals to and from equipment in the IDEEA station pass through the IDEEA interface to the M18 computer. All data transfer and control signals are originated by the computer and all data is processed through the computer. The interface provides the electronics and connections necessary to achieve compatability between systems elements. A total of 61 lines (Table I)* interconnects the interface to the computer. The interface chassis (Figure 9) is composed of the ACT card rack, six circuit cards containing the interface electronics, three power supplies, and nine military type connectors.

An important function of the interface electronics is expansion of the output control signals of the M18 computer. The M18 has only six discrete output lines (OPL lines) which are insufficient to control all the devices in the IDEEA station. The M18 OPL lines can only be selected one at a time, and are subsequently turned off by selection of another OPL line. However, by using one OPL line and four output lines (D-lines) from the M18 (used in transmitting eight-level alpha-numeric or five-level teletype information), a total of 16 new control signals (OPLE lines) is generated.

Through the use of AND and NAND logic, the sixteen possible combinations that can be obtained from the four lines are generated. The M18 OPL5 line in combination with M18 strobe line (FBOO) (which indicates when information is present on the D-line

*Tables I through VI are presented in the Appendix.

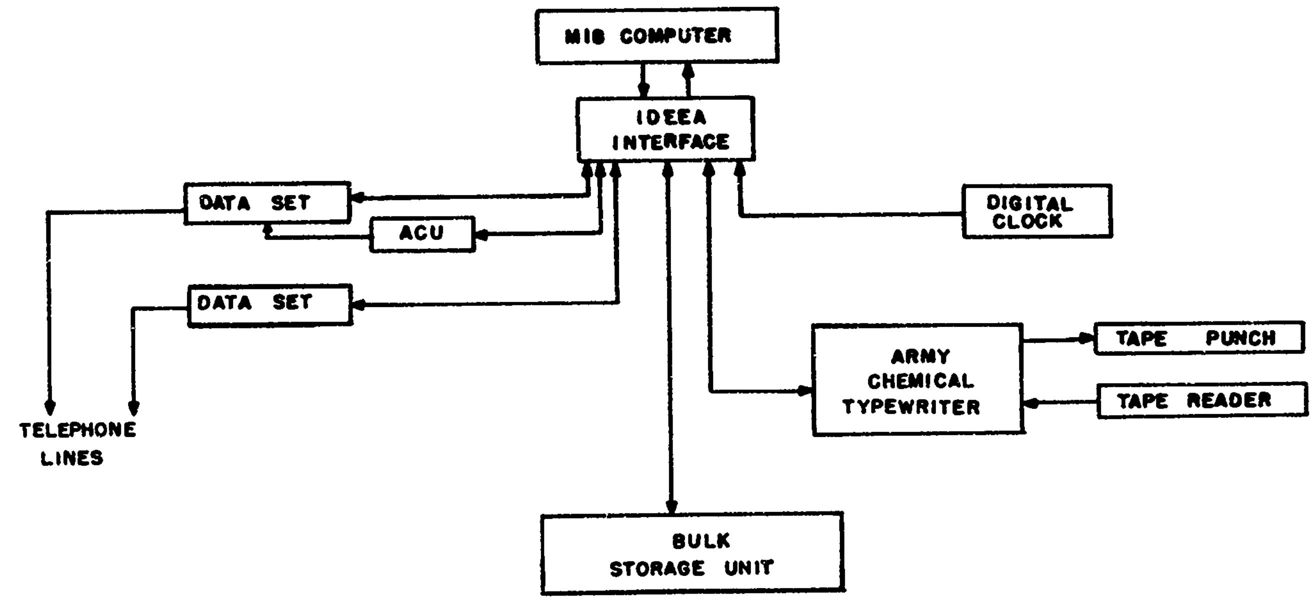



Figure 14. Block Diagram of IDEEA Station

outputs), is used to activate the OPL Extender (OPLE) logic. This is required because the D-line outputs are used to supply data to other pieces of equipment; in fact, some of the OPLE lines are used to determine what piece of equipment is to receive the output signals from the D-lines. For example:

OPLE5 - Activates D-line outputs to the automatic call unit.
OPLE10 - Activates D-line outputs to the ACT.
OPLE12 - Activates D-line outputs to the ACT punch.

An advantage of the OPLE lines over the computer-generated OPL lines is that activation of another OPLE does not turn off previously selected OPLE's. An OPLE can only be turned off by again generating its logic code or by generation of an OPLE15, which resets all the OPLE lines with the exception of OPLE8 and 9. OPLE8 and OPLE9 are used to set and reset the two 103A2 data sets. The functions and logic codes for the OPLE's are listed in Table II. The logic diagram for the generation of the OPLE signals is presented in Figure 15.

## Data Transfer from ACT to M18 Computer

Signals to the M18 from the ACT are in 8-level binary form. The alpha-numeric, control, and special character coding used by the ACT can be found in Table III. Typewriter connections to the interface chassis and the associated computer terms are listed in Table IV.

Typewriter data signals are generated either by keyboard or punched paper tape reader. Data exchange from the ACT to the M18 computer is in parallel form, using nine lines - eight data lines and one strobe line. The strobe line is used to tell the computer that signals are present on the data lines.

The interface circuits for signals from the ACT are level changers, required because of the differences in logic levels. A logical "one" in the ACT is +12 volts pulsating D.C., while a logical "one" to the M18 computer is $-3 \pm 1$ volts. A logical "zero" for both the ACT and the M18 is zero volts.

Data signals from the typewriter are obtained from either the punch or reader coils, depending upon the mode of operation. If the reader is used, the relay bank mounted on the rear of the interface chassis (Figure 9) is automatically switched to allow direct input from the reader coils. By using the reader as the means of data transfer there is no need for a paper tape to be punched and, also, data transfer is faster. The punch or reader clutch provides the timing (or strobe) signal to the computer.

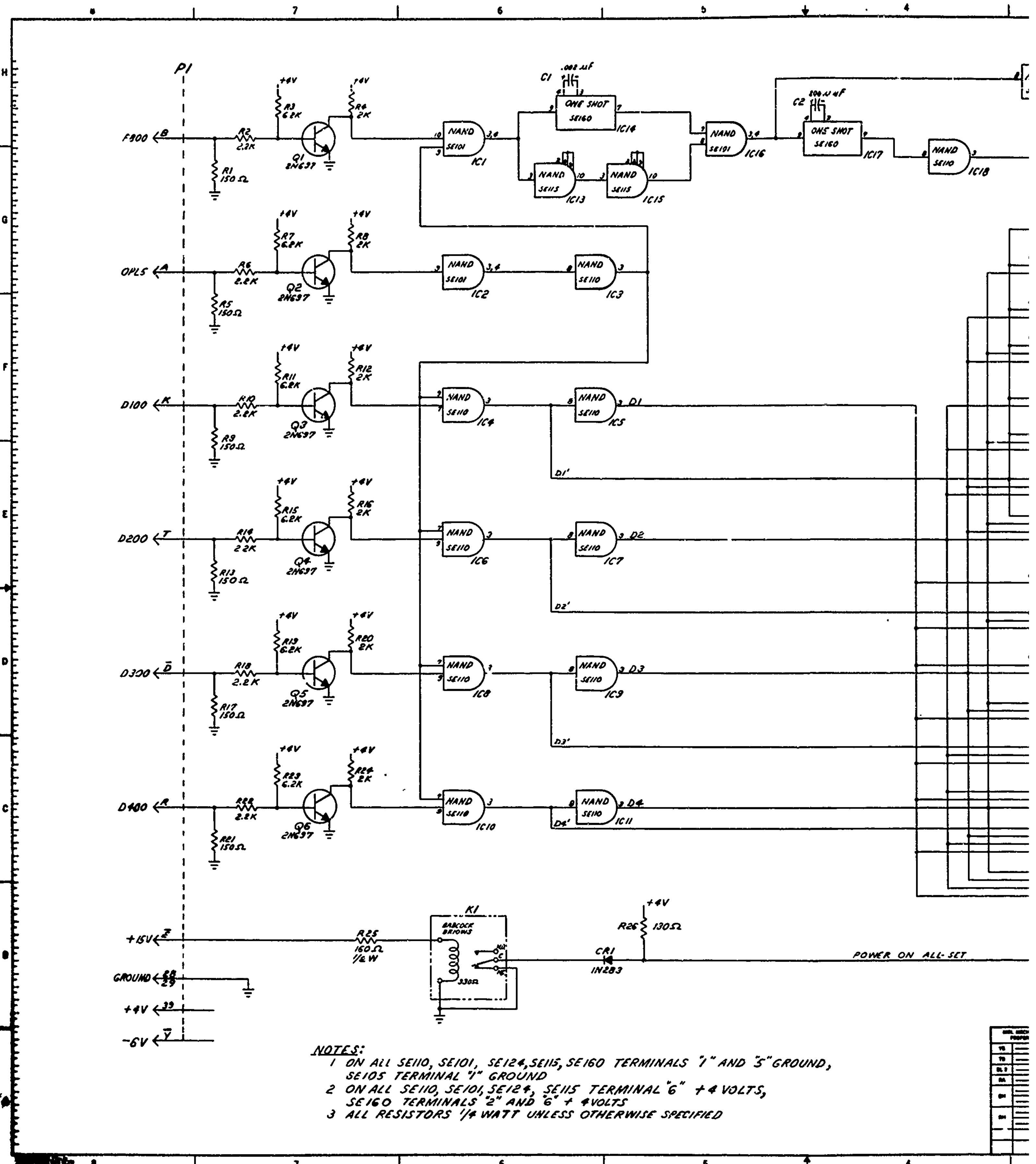
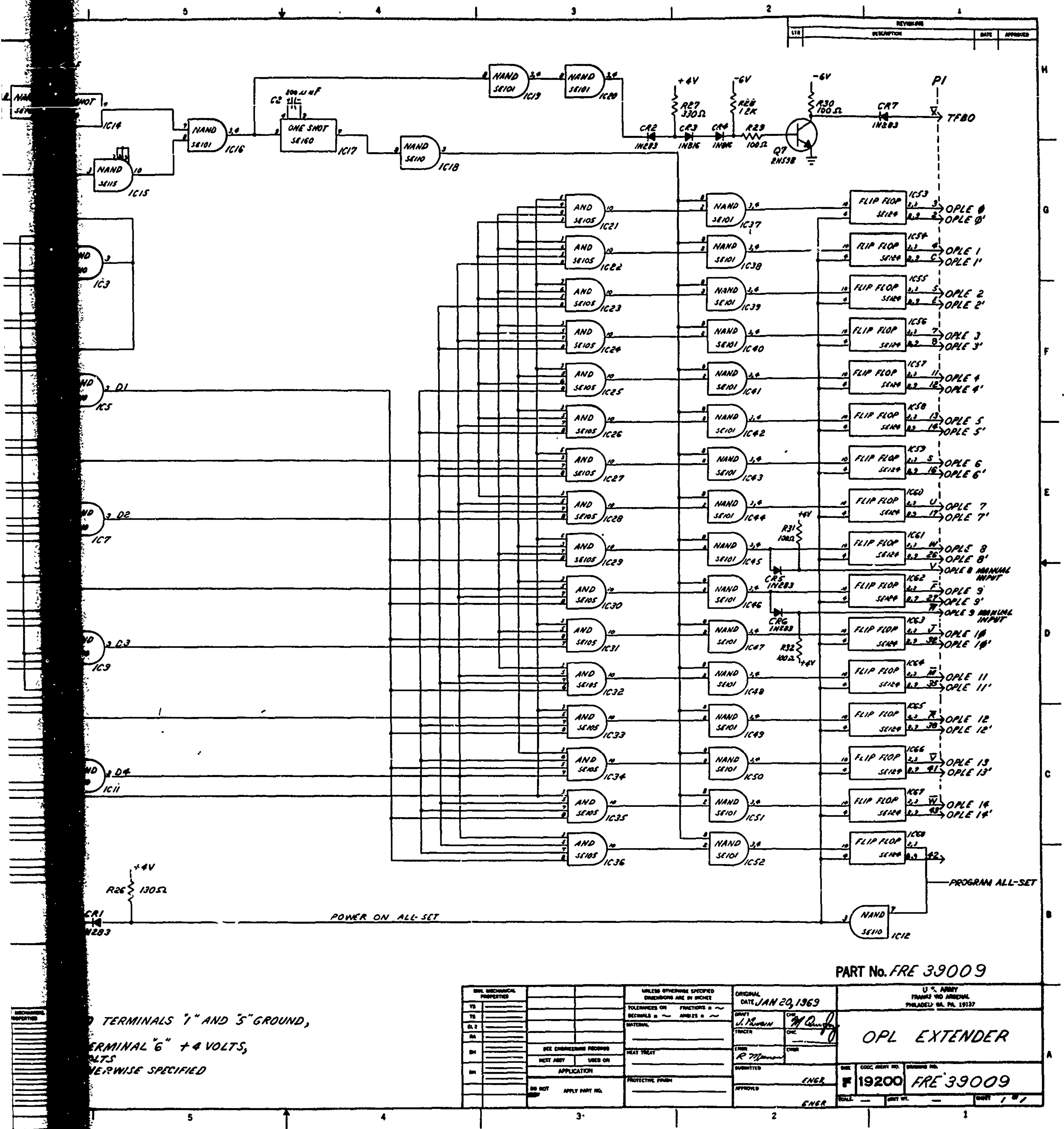



Figure 15. OPLE logic Diagram



PART No. FRE 39009
OPL EXTENDER
U.S. ARMY
FRANKFORD ARSENAL
PHILADELPHIA, PA. 19137
ORIGINAL DATE JAN 20, 1969
F 19200 FRE 39009
TERMINALS "7" AND "5" GROUND,
ERMINAL "6" +4 VOLTS,
OLTS
ERWISE SPECIFIED
POWER ON ALL-SET
PROGRAM ALL-SET
TFBO
OPLE 8 MANUAL INPUT
OPLE 9 MANUAL INPUT


ram

2

Data signals from the ACT are input to the computer through the interface and via the M18 F-lines for manipulation and storage. F-line inputs are sampled into the "A" register under program control. The M18 I-lines (data input lines) are not used because only six of the eight I-lines are data lines - bit seven is a control bit, and bit eight is a parity bit.

Data is read only during the period that the strobe is a logical "one" or -6 volts. As shown in Figure 16, the strobe is located within the middle portion of the data pulse. This assures that when the data pulse is read it has reached its proper signal level.

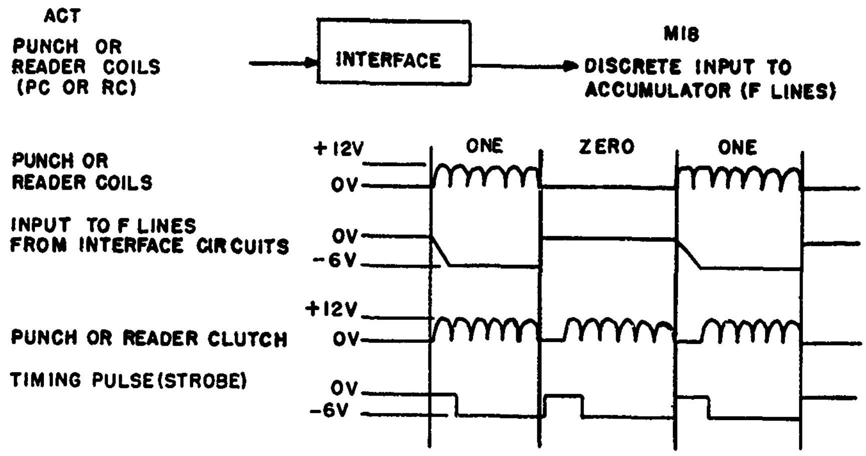



Figure 16. ACT to M18 Computer Signal Diagram

## Data Transfer from M18 Computer to ACT

Data signals from the M18 computer are in eight-level parallel form. The M18 uses ten lines for data transfer - eight data (D) lines, one strobe (FBOO) line, and one feed back (TFBO) line. The eight D-lines (D100 - D800) are M18 output lines used in transmitting eight-level alpha-numeric or five-level teletype information. The strobe line indicates when information is present on the output lines. The feedback is an input to the M18, generated by an external device (in this case the interface) to indicate that data has been accepted.

The computer-to-ACT interface circuits consist of a nine-input register and associated relay drivers and relays. The register functions both as a holding device and a means for level shifting. By using the register to hold data signals, the computer is free to perform other tasks during the much slower mechanical action of the typewriter. The register frees the computer for approximately 100 milliseconds between typed characters, and longer for control characters such as carriage return, line advance, etc. The register was incorporated for use in character by character data transfer over data phone lines. During the 100 milliseconds the computer is free from output duties, it accepts serial input from the data phone, stores the data received, and prepares it for subsequent parallel output to the ACT.

The signals from the register activate associated relay drivers and relays. The relays are used to switch the ACT-generated pulsating D.C. voltages, which activate their respective translator and select reader contacts to produce the mechanical action necessary to provide a character typeout on the ACT.

Output logic levels from M18 D-lines are -6 volts D.C. through 150 ohms (logical one), and -6 volts through 100K ohms (logical zero). The ACT uses a floating ground system, which is +50 volts with respect to the interface ground. The logic levels for the ACT translator circuits are + 12 volts pulsating D.C. for logical one and zero (0) volts for logical zero, but measure +62 and +50 volts, respectively, with respect to interface chassis ground. The logic levels for the select reader circuits in the ACT are -12 volts pulsating D.C. for logical one and zero volts for logical zero, but measure +38 and +50 volts, respectively.

The operations involved in data transfer can be seen in Figure 17. The M18 sets up data levels on the D-lines. The register accepts the data and holds it. The register energizes and holds the associated relay driver circuits, causing the associated relay contacts to close. The M18 generates a strobe pulse (FBOO). The strobe pulse is used to energize a relay which, when selected, applies voltages to contacts for both the translator and select reader coils, as well as their respective clutches.

The strobe is also used to generate the feedback (TFBO) pulse which tells the computer that the register has accepted the data. This frees the computer from output duties and permits it to perform other tasks while the register holds the output data. The register is reset when the ACT-generated inhibit pulse is removed. The inhibit pulse is present during the entire time required to mechanically type a character or perform a typewriter function.

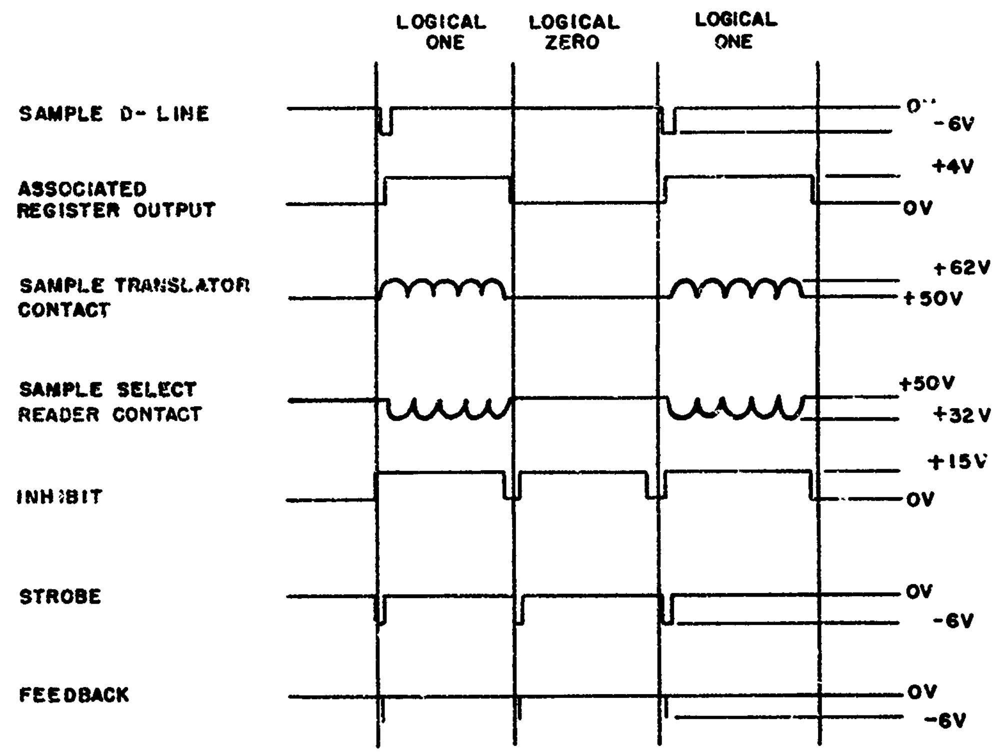



Figure 17. M18 Computer to ACT Signal Diagram

## Data Transfer from Digital Clock to M18 Computer

The digital clock and the ACT time share the same eight F-line inputs to the M18 computer. Unlike the ACT, the digital clock requires no level-changing circuits since logic levels for both the clock and the M18 are -3 $\pm$ 1 volt, logical one and zero volt, logical zero. Data flow is from the clock to the computer, with only a single control signal (Activate-Feedback signal, OPLE6) from the M18 to the clock. As shown in Figure 18, the computer supplies an activate-feedback signal to the clock when it wants to read the time. The activate-feedback line is used both as a signal to set up data and as a signal that data has been received and the next two digits are to be set up on the data lines.

Signals are output in series-parallel form, using a strobe feedback concept. There are eight data lines, one strobe line, one activate-feedback line, and a ground line. All data appears over the same eight data lines. Data appears in groups of two digits, starting with seconds, followed by minutes, hours, and days. The time outputs are in 8-4-2-1 binary-coded decimal form, and a complete time reading is supplied to the computer in less than one second.

The strobe line has a true level placed on it when data is present on the data lines. This level is removed immediately upon receiving a feedback pulse and appears again when data is present. This procedure is repeated until all data is stored. The last feedback pulse deactivates the clock outputs.

Digital clock interconnections and associated computer terms are listed in Table V.

Dual output connectors are provided to allow hookup with either positive or negative logic computers. A total of sixteen data lines, eight each for connectors J18 and J19 respectively, are supplied. In addition, each connector has one activate-feedback line, one sample-data line, one strobe line, and a ground. Data appears at both output connectors simultaneously. Logic levels for J18 are +4 $\pm$ 1 volt for true (1), 0 + 1 volt for false (0). For J19, logical true (1) is -6 + 1 volt, and logical false (0) is zero volt.

## Data Transfer between Disc Memory Unit and M18 Computer

The disc memory unit interacts with the M18 computer through its own controller interface. Interconnections between the controller interface and the M18 are listed in Table VI.

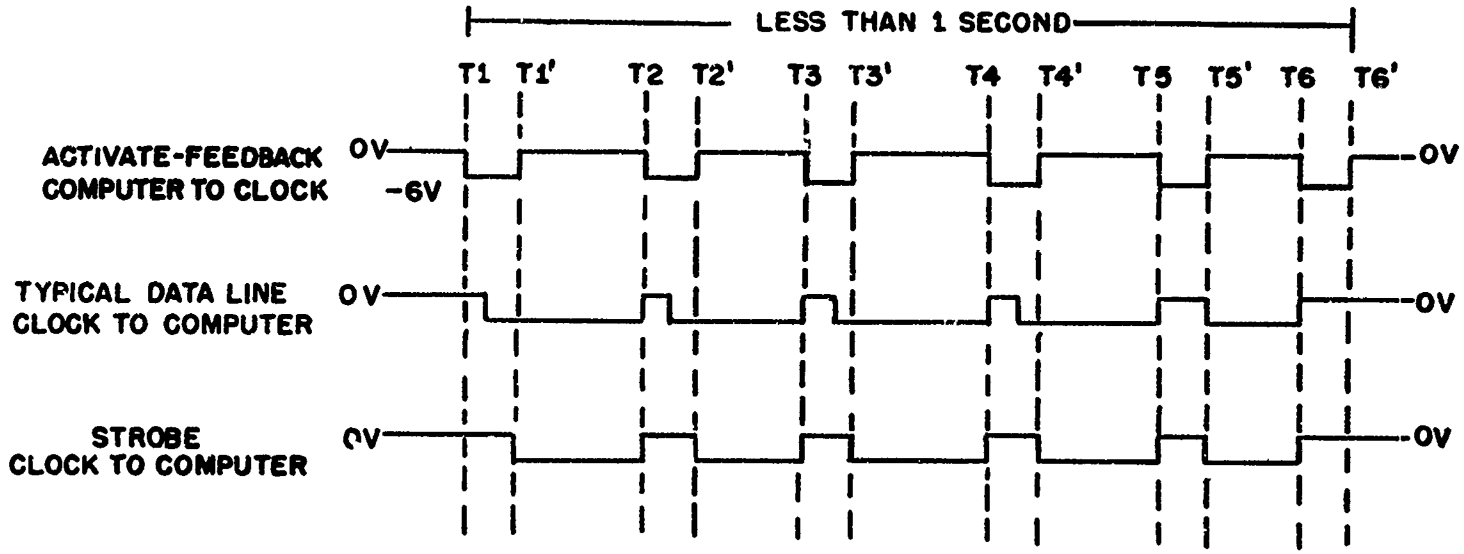



Figure 18. Digital Clock Signal Diagram

The controller directs the functions of head selection and change, data reading, and data writing. The disc provides timing information in the form of track origins, sector clocks, read/write clocks, and status information such as Disc Ready, Read Error, and Read Inhibit.

Data and commands are transferred from the M18 to the bulk storage unit via the M18 output lines (D lines). Signals to the M18 from the disc are applied to the computer's 8 input (I) lines and the strobe term if TG. The FBIO term, as in the other data transfer operations, provides the feedback signal. The M18 MTF logic term is used to put the controller into either the input or verify mode of operation. The RGO signal, when on, indicates that the M18 is in the input by external device mode for machine controlled I-line input.

Commands from the M18 are transmitted as three 8-bit characters, two for track selection and one for supervision of data transfer. These characters are accepted by the M18-disc interface, level-shifted to integrated circuit logic levels, and then stored temporarily in an 8-bit character buffer. The first and second characters are combined and loaded into bits 1-16 of the 32-bit assembly/disassembly buffer, from which they are transferred to the appropriate subchannel to begin track selection. The third command character, when received, is held in the assembly/disassembly buffer until track selection is completed (up to 740 milliseconds). The third character is then transferred into the disc controller to supervise data transfer. Data transfer is initiated by the M18 transmitting a command word to the disc controller. The following is the format of a command word.

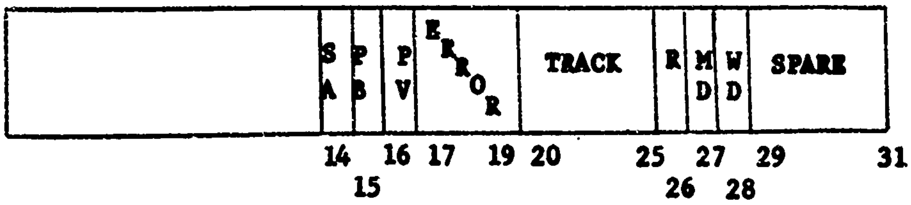
Command Word Format

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | UNIT | TRACK ADDRESS | SECTOR ADDRESS | R/W | RP | POV | SECTOR COUNT | |
| 0 | 1 | 2 7 | 8 14 | 15 | 16 | 17 | 18 23 | 31 |
| | 1st character | | 2nd character | | | 3rd character | | |

| Character (Alpha 4) | Bit Position | Content |
|---|---|---|
| 1st | 0-1 | Disc unit number<br>Range: $00_2$ - $11_2$ |
| | 2-7 | Track address<br>Range: Track 0 to $63_{10}$ (0 - $77_8$) |
| 2nd | 8-14 | Sector address<br>Range: Sector 0 to $127_{10}$ |
| | 15 | R/W bit<br>Read - 0<br>Write - 1 |
| 3rd | 16 | RP bit - must be set in order to change the protect/unprotect indicator for a record. This indicator is physically located on the disc at the beginning of each record. |
| | 17 | POV bit - used in combination with the unprotect switch on the disc control panel to override the protected status of a record and enable writing. |
| | 18-23 | Sector Count - This count determines the number of sectors to be read or written. Range: 1 to $64_{10}$. A sector count of 0 is equivalent to $64_{10}$. |

A maximum of 1024 M18 words can be transferred by one input/output command. This is equivalent to sixty-four 16-word sectors on the disc. It is mandatory that a status word be obtained after each data transfer to insure error-free operation. Status information is received from the disc controller and loaded into bits 1-16 of the assembly/disassembly buffer. From there it is disassembled into two 8-bit characters which are transferred individually to the 8-bit character buffer and from there to the M18 computer. The format for status information follows.

Status Word Format




| Bit Position | Meaning |
|---|---|
| 0-13 | Not used |
| 14 | SA: Sector Available - If set to a "1," then the next sector is immediately accessible for subsequent I/O. This bit can be ignored since M18 is not fast enough to utilize this capability. |
| 15 | PB: Protect Bit - This bit indicates if a record is protected or unprotected. If more than one record is accessed during the I/O operation, PB will be set if any of the records accessed is in the protected state. |
| 16 | PV: Protect Violation - This bit is set if a write operation is attempted on a record which is in the protected state. |
| 17-19 | Error - The following are the error conditions: |

000 - No error

001 - Parity error from M18 to controller

010 - Cyclic Redundancy Error on data from disc to controller. A CRC character is written at the end of each sector during writing. This character is generated from the data recorded on the sector. During reading, a CRC character is generated and compared with the one recorded at the end of the sector.

011 - Controller Procedure Error. This error occurs under the following conditions:

| Bit Position | Meaning |
|---|---|
| | a. Read a word during a write operation.<br>b. Write a word during a read operation.<br>c. Execute an I/O operation after an error has occurred without first reading a status word.<br><br>100 through 111 are meaningless when employed with M18. |
| 20-25 | TRACK: The last track accessed during the previous I/O operation. |
| 26 | R: Ready bit - not used. |
| 27 | MD: Missing Data. This bit is set if the words transferred by the I/O command are less than the words specified in the sector count of the command word.<br><br>If the above conditions exist on a write operation, the disc area associated with the words not transferred by the output command is cleared to zero. Therefore, if one word is output and the sector count equals 1, the last fifteen words of the sector addressed are cleared to zeros. |
| 28 | WD: Write Disable - This bit is set if the write disable switch on the disc unit is depressed. |
| 29-31 | Not used. |

M18 computer words are transferred to (from) the disc system in alpha 6 mode. Each character consists of 6 data bits plus a parity and a control bit. As each character is received (transmitted), the parity and control bits are stripped off (regenerated) in the 8-bit character buffer.

In write operations, the remaining 6 data bit characters are, in turn, formatted into the 32-bit assembly/disassembly buffer (the four synchronization bits in the first character are not transferred). Each 32-bit M18 data word thus formatted is stored as two 16-bit half-words in successive locations in the Buffer Memory. When sixteen M18 words have been loaded into the memory, it will signal the basic controller to begin writing on the disc.

Data to be written on a disc is read from the buffer memory in 16-bit half-words and transferred in parallel to the Serial Data Register. From here it is shifted, a bit at a time, out to the selected subchannel controller. As the data is shifted out, the cyclic redundancy check (CRC) character is computed. After 32 half-words have been written on the disc, the cyclic check character resulting from the computation is shifted out and recorded, thus completing the Sector. The Sector Counter is decremented by one, and if non-zero, a request for another sector of data from M18 is made to the buffer and interface logic. When data is read from the disc, it is shifted serially into the serial data register. Concurrently, the data is used by the redundancy check logic to compute the check character. After each half-word is received in the serial data register, it is transferred in parallel to the assembly/disassembly buffer for temporary storage in the buffer memory.

## Signals between M18 Computer and 103A2 Data Sets

Interface circuits permit logical interaction between the M18 computer and both the 103A2 data sets. Data set logic functions and systems operation are explained with the aid of Figure 19.

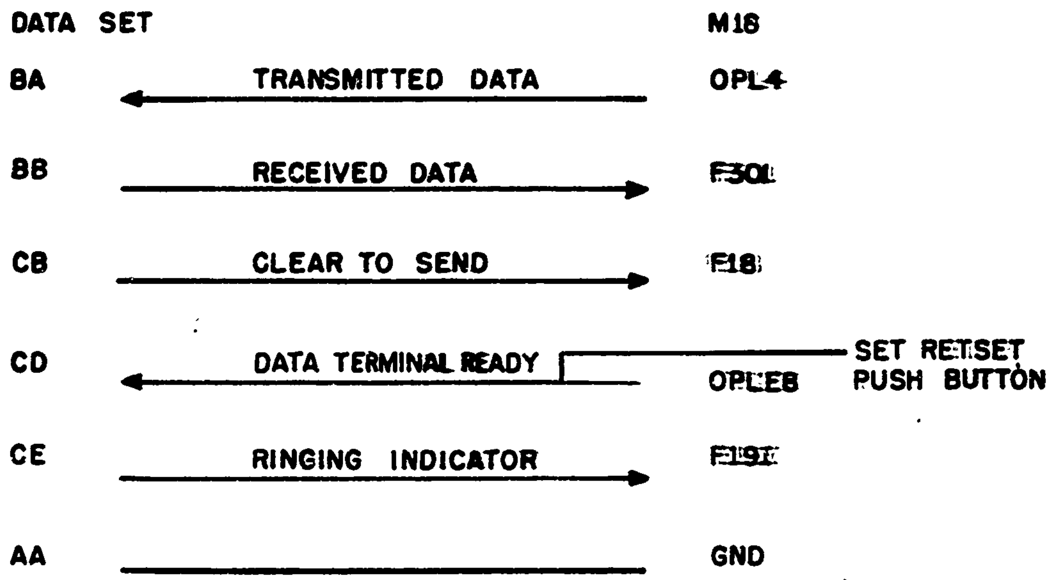



Figure 19. M18 Computer-103A2 Data Set Signal Lines

BA (transmitted data) is used by the M18 to present the data to be transmitted. It is only operative when circuit CB (clear to send) is ON. BB (received data) delivers the data received by the data set M18. CB (clear to send) indicates to M18, when ON, that the data set has established a connection with the distant data set and that signals may be applied to circuit BA (transmitted data). CC (data set ready) indicates, when ON, that the data set is in the data mode; that is, it is not in the idle, talk, test, or local condition, nor is it without power. CD (data terminal ready) is used by the M18 to permit the data set to enter and remain in the data mode.

The yellow push-button light switches on the front panel of the interface chassis can be used to manually set or reset the CD (data terminal ready) logic function. CE (ringing indicator) turns ON to indicate the receipt of a ringing signal by the data set. If all conditions for automatic answering are met, it will turn ON for a brief period when the call is answered. If automatic answering is not enabled, the ON indication follows the ringing cycle. Another signal CF (carrier detector), when ON, indicates that data carrier is being received from the distant end and is used by the data set only.

Before a telephone connection has been established, the IDEEA station has circuit CD (data terminal ready) ON. The originating station dials another station either manually or automatically, and the answering data set is automatically placed in the data mode by the computer or by manually depressing the "DATA" key on the telephone instrument after an interval of voice communication. As the answering set enters the data mode, its circuit CC (data set ready) comes ON and its "DATA" key is illuminated. A tone is sent back to the originating station and is heard by the person placing the call or the ACU (automatic calling unit). The data set is then placed in the data mode by operation of its data key or by an electrical signal from the ACT. Circuit CC at the originating station comes ON, and its DATA key is illuminated. After 200 milliseconds, CB (clear to send) and CF (carrier detector) on the originating set turn ON. At this time the send circuit is placed under control of the data on circuit BA. The answering set turns its circuits CB and CF ON and puts its send circuit under control of the data on the circuit, BB.

## Signals between M18 Computer and Automatic Call Unit

The data auxiliary set 801 automatic call unit (ACU) permits the M18 computer to originate data-phone calls automatically. Control signals and the number to be dialed are passed between the M18 and the ACU in the form of binary electrical signals. Digits to be dialed are presented to the ACU, one at a time, in four-lead binary form.

As each digit of the telephone number is dialed, the ACU requests the next digit from the M18 until dialing has been completed. Interconnection and ACU term descriptions are shown in Figure 20 and are described in the following paragraphs.

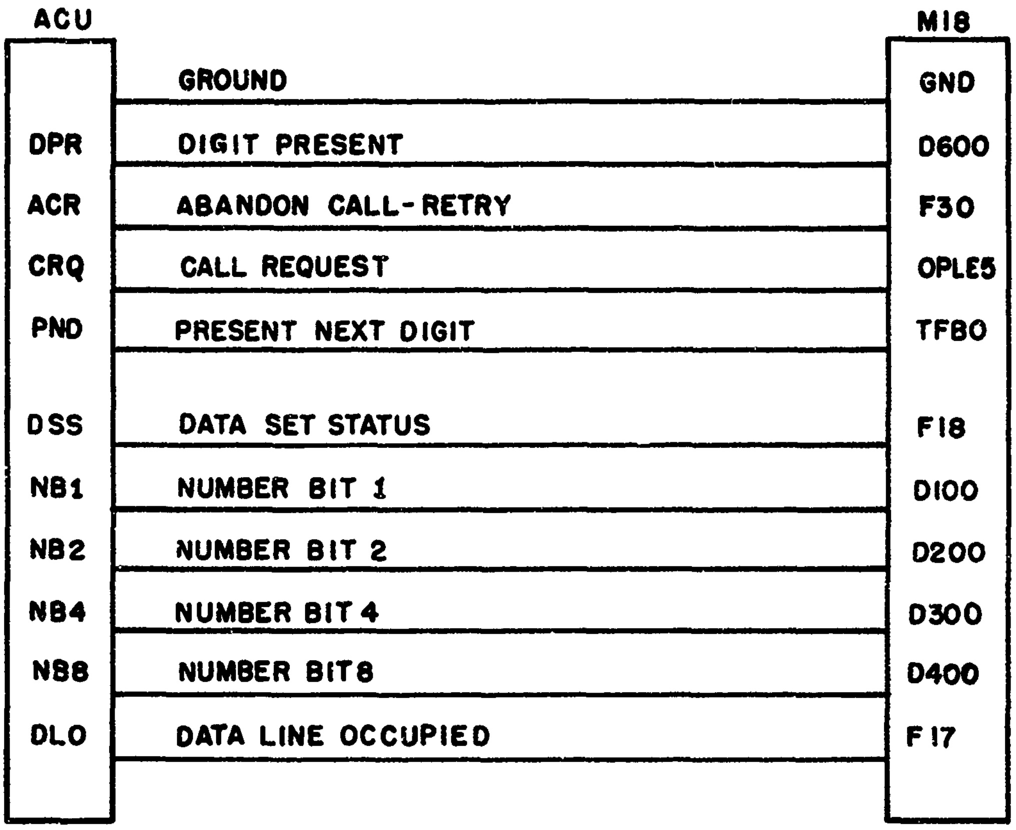



Figure 20. M18 Computer-ACU Signal Lines

A call request (CRS) signal is generated by the M18 to request the ACU to originate a call. The ON condition indicates a request to originate a call and must be maintained during the complete call origination period in order to hold the communication channel "off-hook." The OFF condition indicates that the M18 has completed its use of the automatic calling equipment. Parallel binary signals on the digit leads (NB1, NB2, NB4, NB8) are generated by the M18, causing the ACT to produce the desired digit dialing signals. The binary codes for the digits to be dialed follow.

Digit Lead Coding

| | Number | | | |
|---|---|---|---|---|
| | D400 | D300 | D200 | D100 |
| Digit | NB8 | NB4 | NB2 | NB1 |
| Value | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |

The Digit Present (DPR) signal is generated by the M18 to indicate that the ACU may now read the code combination presented on the digit leads NB1, NB2, NB4, NB8. The ON condition indicates that the M18 has set the states of the digit leads.

Present Next Digit (PND) signals are generated by the ACU to control the presentation of digits on the digit leads. During dialing, the ON condition indicates that the ACU is ready to accept the next digit indicated on leads NB1, NB2, NB4, and NB8. The OFF condition indicates that the M18 must turn DPR (digit present) OFF and set the states of the digit leads for the next digit. After the M18 turns DPR (digit present) OFF following presentation of the last code combination on the digit leads, PND (present next digit) comes ON and remains ON.

Data Line Occupied (DLO) signals are generated by the ACU to indicate the communication channel is in use for automatic calling, data communication, voice communication, or testing of the automatic calling or data communication equipment. Data Set Status (DSS) signals are generated by the ACU to indicate the status of the data communication equipment. The ON condition indicates that the telephone line is connected to the data set to be used for data communication and that the data set is in the data mode. Abandon Call and Retry (ACR) signals are used to indicate that a preset time has elapsed since the last change of state of PND

(present next digit). The ON indication is a suggestion to the M18 to abandon the call and try again later if the connection has not yet been completed. The ACU does not abandon the call when this lead is turned ON.

## Multicomputer IDEEA Station

The IDEEA station at Frankford Arsenal is similar to the other network stations with the exception that a Systemizer has been incorporated. The Systemizer (Figure 21) is a device which allows up to seven M18 computers, two bulk storage units, three serial data devices, two automatic call units, two parallel data devices, and one signal data reproducer AN/GSQ-64 (MLU) to be used in a single computing system. For information transfer between member devices, interconnections can be established under program control by one of the computers (the Executive) or under manual control by means of a push-button matrix on the front panel of the systemizer.

All system devices are connected to the rear panel of the systemizer. A relay tree is used to control the various connections that are made. The systemizer front panel contains a display which shows the devices not presently hooked up to other devices in the system, a display of interconnections that are in effect at any time, and buttons which allow the system operator to manually connect or disconnect combinations of system devices.

The systemizer is put into the manual mode by depressing the "manual" button. A hookup between two devices is achieved by depressing the button located in the proper row for the first device and the proper column for the second device. The area surrounding the button becomes lighted (red), and the corresponding "Device Ready" indicators (green) are extinguished. The indicators remain in this condition until the hookup is broken by again depressing the same button.

The systemizer is put into the automatic mode by depressing the "auto" button. In the automatic mode of operation, computer No. C1 performs the functions of monitor and control of the overall system. It exercises network control by directing the systemizer to accomplish "hookups" as required by an executive program. It monitors the status of the network by sampling its discrete input lines for "ready" signals which correspond to each of the other devices in the system. A "true" M18 logic level on the following F lines indicates to C1 that the corresponding device is "ready" to be hooked up.

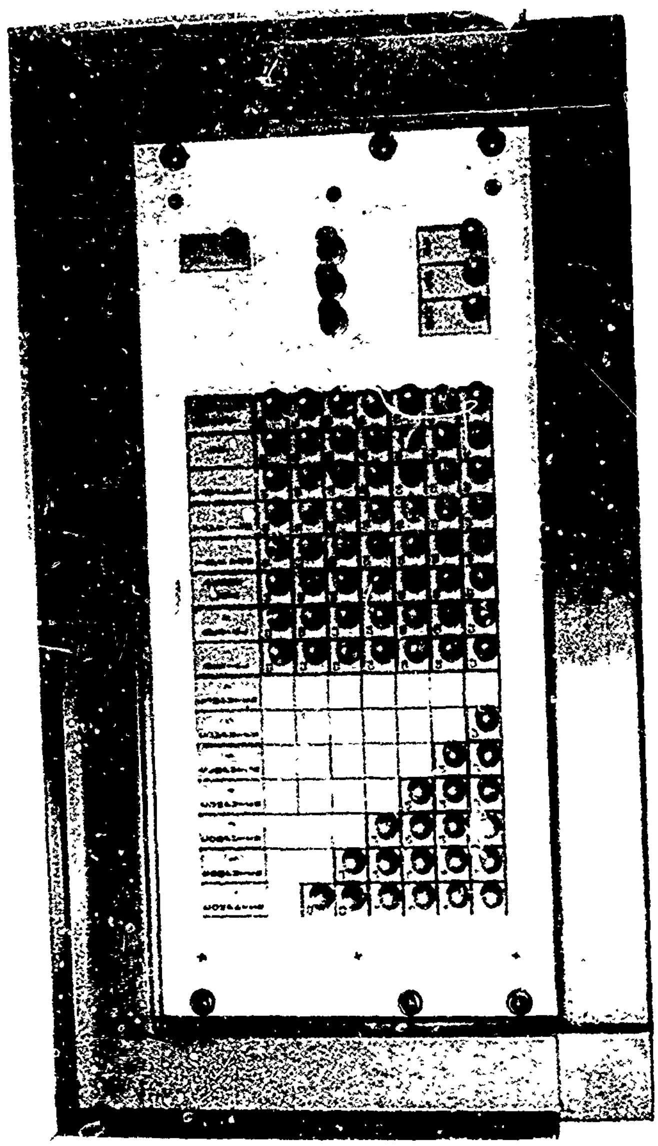


Figure 21. Systemizer

| DIA* POSITION | M18 TERM | DEVICE |
|---|---|---|
| 3 | F29I | C2 M18 computer |
| 4 | F38I | C3 M18 computer |
| 5 | F27I | C4 M18 computer |
| 6 | F26I | C5 M18 computer |
| 7 | F25I | C6 M18 computer |
| 8 | F24I | C7 M18 computer |
| 9 | F23I | T1 bulk storage unit |
| 10 | F22I | T2 bulk storage unit |
| 11 | F21I | P1 parallel input/output device |
| 15 | F17 | S2 data phone or serial I/O device |
| 16 | F16 | S3 data phone or serial I/O device |
| 17 | F15 | S1 data phone or serial I/O device |
| 18 | F14 | P2 ACT |

No "ready" signal is needed for the MLU.

When the system is operating in the automatic mode, ringing signals from 103A2 data sets connected to S1, S2, and S3 are supplied to C1 in particular bit positions of its "A" register. C1 determines which computer (any available satellite or C1 itself) will receive the call and connects the selected computer to the data set. The ringing signal is detected by the receiving computer in one of the bit positions of its "A" register. The receiving computer addresses the 103A2 by setting its OPL6 discrete output line "true," then "false" again. This causes an "answer" signal to be supplied to the data set and the yellow "set-reset" on the front panel of the systemizer lamp for the corresponding serial device goes out. A "clear-to-send" signal from the data set is supplied to the receiving computer in another bit position of its "A" register. Serial data is output by the connected computer via its OPL4 discrete output line. Serial data is received by the connected computer via a third bit position of its "A" register. The data set is de-addressed by the connected computer by again setting its OPL6 line "true" and then "false;" this causes the "answer" signal to be removed from the data set and the corresponding "set-reset" lamp to glow yellow again.

*DIA - Discrete input to accumulator.

## OPERATING EXPERIENCE AND CAPABILITIES

The IDEEA stations were designed to provide a means for gaining access to automated information files. To date, experience with the IDEEA stations has been limited by a lack of suitable information files. However, the IDEEA console has been used with the CIDSII (multiterminal) information system which has automatic on-line retrieval capability for chemical information, including structures.

IDEEA stations at Frankford Arsenal and Edgewood Arsenal have been used to query the chemical structure data bank located at the University of Pennsylvania. Inquiries to the data bank are entered through the ACT keyboard or tape reader and sent through data sets over phone lines to the data bank, and responses are received over the phone lines and are output as either typewritten hard copy and/or a paper tape.

Responses from the CIDSII data bank are in USASCII code or a 7-bit information code utilized by a commercial typewriter. USASCII code characters are recognized by the army chemical typewriter and a hard copy output is produced. All chemical structures are output on paper tape and can subsequently be used to obtain a typewritten hard copy of the chemical structures requested.

Experience has shown that the capabilities of the IDEEA station would be greatly increased by replacing the M18 computer and the army chemical typewriter with new units and by using higher bit rate telephone data sets.

Replacement of the M18 computer by a new state-of-the-art small scale computer would increase the speed and control capabilities used in retrieving, processing, receiving, and transmitting information. The M18 computer is limited in both input-output capabilities and control functions. New multiaccess computers permit multiple hookups, faster processing, transmitting, and receiving of information. Current commercial computers are capable of operating at speeds of two magnitudes greater than the M18. Multiaccess computers permit establishment of interrupts, and permit direct interfacing of peripheral hardware.

Another major reason for replacement of the M18 is the problem of obtaining required software. Programming personnel, familiar with the working of the M18, are limited. Considerable experience is required in order to be able to write operational programs for the M18 due to the limited number of programming aids available. Programs, such as input/output over phone lines where timing is important, can only be handled by personnel with vast M18 programming experience.

The M18 has two assemblers but has no operating compiler. A commercial computer would have available symbolic assemblers and would permit the use of high language (Algol, Fortran IV, etc.) compilers. The use of these aids would make the development of software a much more manageable task.

Experience has also shown that the ACT is unsuitable as an information system input-output device. The ACT is both mechanically slow and unreliable, as are most typewriter devices. The replacement for the ACT should be data-phone interfacable, solid state, reliable, and systems-oriented.

A more suitable type device for an information retrieval system would appear to be one that uses a cathode ray tube display. These devices have little or no mechanical problems and most of these devices are capable of handling data from high speed data sets. Data retrieval by this type device is extremely fast; however, a [redacted] line printer or other special equipment is required to produce a hard copy output.

High speed data sets that handle over 2000 bits/sec are available. These data sets would permit higher data transfer rates than the present data sets.

A series of experiments using the IDEEA stations should be devised. The purpose of these experiments would be to determine the users' needs in the field of information retrieval. By obtaining the users' needs, useful and effective data retrieval methods could be studied. These experiments should offer alternative methods and formats for obtaining information to determine the most desirable and efficient means of information retrieval. In addition, the IDEEA network could be used to study the advantages and disadvantages of having a computer processor unit contained in each retrieval station.

The advantages of a computerized system are numerous. An automated station could be preprogrammed to allow a multiplicity of information queries to be handled swiftly, automatically, and ordered in any desired manner. The system may be left unattended during nonworking hours, making queries, receiving data, answering any queries made into its own data bank, and channeling information received to the desired output device. Another major advantage is that the computerized station could be programmed to conduct a dialogue with the user to guide him in the preparation of his query into the proper coding and format for submission.

## CONCLUSIONS

1. The IDEEA Console provides a means for gaining access to automated technical information networks. The consoles should be used for this purpose and data collected.

2. For the IDEEA Network to be useful, suitable data banks and interested users must be obtained. At present, no large scale usable data banks exist.

3. The performance of the IDEEA Station could be greatly increased by updating equipment used in the stations.

## RECOMMENDATIONS

It is recommended that

1. All available automated information retrieval systems be studied and evaluated to determine the complexities and problems involved in information retrieval and to investigate the possibility of using the developed IDEEA Stations with these systems.

2. The IDEEA Station capabilities be upgraded to increase reliability, speed, and versatility of the system.

3. A study be conducted to determine the usefulness of commercially available information retrieval system devices.

## APPENDIX

## TABULATED DATA

Tables I through VI present detailed data as follows:

TABLE I. IDEEA Interface-to-M18 Computer Interconnections and Term Descriptions

| M18 Pin No. | Interface Pin No. J44 | M18 Term | Description |
|---|---|---|---|
| P10-A | | | Not used for IDEEA. |
| P10-B | | | |
| P10-C | | | |
| P10-D | | | |
| P10-E | | | |
| P10-F | | | |
| P10-G | | | |
| P10-H | | | |
| P10-J | P44-A | D100 | Output lines from GDC, M18 transmitting 8-level alpha-numeric or 5-level teletype information. |
| P10-K | P44-B | D200 | |
| P10-L | P44-C | D300 | |
| P10-M | P44-D | D400 | |
| P10-N | P44-E | D500 | |
| P10-P | P44-F | D600 | |
| P10-R | P44-G | D700 | |
| P10-S | P44-H | D800 | |
| P10-U | P44-NN | IMTØ | Output from M18. This normally false term is true during a/n 5, a/n 4, and decimal output modes. |
| P10-V | P44-J | FDØØ | This M18 output term indicates when information is present on the output lines: D100 through D800 |
| P10-W | | | Not used for IDEEA. |
| P10-X | P44-K | ØPL1 | Discrete output lines. OPL1 is activated by operation code 3702, OPL2 by 3704, and OPL3 by 3706. Only one OPL may be selected at one time. Selected OPL will be turned off by subsequent selections of another OPL, or by the DOF (3700) command. |
| P10-Y | P44-L | ØPL2 | |
| P10-Z | P44-M | ØPL3 | |

TABLE I (Cont'd)

| M18 Pin No. | Interface Pin No. J44 | M18 Term | Description |
|---|---|---|---|
| P10-/A | | | |
| P10-/B | | | |
| P10-/C | | | Not used for IDEEA. |
| P10-/D | | | |
| P10-/E | | | |
| P10-/F | P10-/J | TFAI | Inputs to M18. These terms are feedback signals from some external device. |
| P10-/G | | | Not used for IDEEA. |
| P10-/H | P44-N | TFBØ | Inputs to M18. These terms are feedback signals from some external device. |
| P10-/I | | | Not used for IDEEA. |
| P10-/J | P10-/F | TEØP | An M18 output term that is the inverse of TFBØ. This term is used in conjunction with information output. |
| P10-/K | P44-P | F19I | |
| P10-/M | P44-R | F20I | Input to GDC M18. This term is sampled into the "A" register under program control. A one-to-one correspondence exists between the F subscripts and the corresponding bit positions of the "A" register. |
| P10-/N | P44-S | F21I | |
| P10-/P | P44-T | F22I | |
| P10-/Q | P44-U | F23I | |
| P10-/R | P44-V | F24I | |
| P10-/S | | | |
| P10-/T | | | |
| P10-/U | | | |
| P10-/V | | | Not used for IDEEA. |
| P10-/W | | | |
| P10-/X | | | |
| P10-/Y | | | |
| P10-/Z | P44-PP | PWR GND | Power ground |

TABLE I (Cont'd)

| M18 Pin No. | Interface Pin No. J44 | M18 Term | Description |
|---|---|---|---|
| P10-AA | | | |
| P10-BB | | | |
| P10-CC | | | |
| P10-DD | | | |
| P10-EE | | | Not used for IDEEA. |
| P10-FF | | | |
| P10-GG | | | |
| P10-HH | | | |
| P17-A | P44-W | -3V | -3V regulated supply. |
| P17-B | P44-X | -3V | -3V regulated supply. |
| P17-C | | | Not used for IDEEA. |
| P17-D | P44-/C | 11G | |
| P17-E | P44-/D | 12G | |
| P17-F | P44-/E | 13G | |
| P17-G | P44-/F | 14G | |
| P17-H | P44-/G | 15G | Data input lines to GDC M18 in 8-level alpha-numeric or 5-level teletype. |
| P17-J | P44-/H | 16G | |
| P17-K | P44-/I | 17G | |
| P17-L | P44-/J | 18G | |
| P17-M | P44-/K | TG | An input to GDC M18. This term is used for strobing of the input data lines 11G through 18G. This can be configured in alternate ways. |
| P17-N | | | |
| P17-P | | | Not used for IDEEA. |
| P17-R | | | |

TABLE I (Cont'd)

| M18 Pin No. | Interface Pin No. J44 | M18 Term | Description |
|---|---|---|---|
| P17-S | P44-CC | TE1P | An output from GDC M18. This term is used in conjunction with information input. TEIP is the inverse of the TG signal. |
| P17-T | P44-MM | MTF | An input to M18. With the MTF line open, the M18 is in the "INPUT" mode; ground, in the "VERIFY" mode. |
| P17-U | | | Not used for IDEEA. |
| P17-V | P44-/N | FBIØ | An output from GDC M18, to an input device. This term is normally false. FBIO goes true when the M18 is in the mode to sample the information on the input lines. This signal returns to the false state when TEIP goes true. Maximum information to and from M18 is dependent on the type of information transferred. Maximum rates are:<br>4000 characters per second in a/n 6 mode<br>3500 characters per second in a/n 5 mode<br>500 characters per second in Octal or Decimal mode. |
| P17-W | P44-Y | RGØ | This output signal goes true when FADAC is in an "INPUT EXTERNAL DEVICE" condition. |
| P17-X | P44-Z | RHØ | Inverse of RGØ. When FADAC goes out of the RGØ mode, output term RHØ goes true. |
| P17-Y | | | Not used for IDEEA. |
| P17-Z | | | Not used for IDEEA. |
| P17-/A | P44-/P | ØPL4 | Discrete output lines. OPL4 is activated by operation code 3710, OPL5 by 3712, OPL6 by 3714. Only one OPL may be selected at one time. Selected OPL will be turned off by subsequent selection of another OPL or by the DOF (3700) command. |
| P17-/B | P44-/Q | ØPL5 | |
| P17-/C | P44-/R | ØPL6 | |
| P17-/D | P44-/A | GPRC/ | An input to M18. This term in conjunction with the GPHC/ controls the "RUN-HALT" mode of the computer. With an open circuit, the computer is in the "RUN" mode; with -10.0 ±1V applied, the computer is in "HALT" mode. |

TABLE I (Cont'd)

| M18 Pin No. | Integrated Pin No. J44 | M18 Term | Description |
|---|---|---|---|
| P17-/E | P44-/B | GPHC/ | An input to M18. This term in conjunction with GPRC/ controls the "RUN-HALT" mode of the computer. With an open circuit, the computer is in the "RUN" mode; with +6 $\pm$1V applied, the computer is in the "HALT" mode. |
| P17-/F | P44-/S | FBPR | An input to M18. Initiates octal input when computer is in manual halt mode. Normally false (clamped to 0.0 $\pm$5V) FBPR is -10.0 $\pm$1V when true. |
| P17-/G | P44-/T | F25I | |
| P17-/H | P44-/U | F26I | Inputs to GDC M18. These terms are sampled into the "A" register under program control. A one-to-one correspondence exists between the F subscripts and the corresponding bit positions of the "A" register. |
| P17-/I | P44-/V | F27I | |
| P17-/J | P44-/W | F28I | |
| P17-/K | P44-/X | F29I | |
| P17-/M | P44-/Y | F30I | |
| P17-/N | | | |
| P17-/P | | | |
| P17-/Q | | | |
| P17-/R | | | Not used for IDEEA. |
| P17-/S | | | |
| P17-/T | | | |
| P17-/U | | | |
| P17-/V | P44-PP | PWR GND | Power ground |
| P17-/W | P44-FF | CH GND | Chassis ground |
| P17-/X | P17-/Y | 35V | Not used for IDEEA. |

TABLE I (Cont'd)

| M18 Pin No. | Integrated Pin No. J44 | M18 Term | Description |
|---|---|---|---|
| P17-/Y | P17-/Z | 35V1 | These voltages energize the appropriate write switches allowing the computer to write into "COLD" storage and, therefore, all 8,192 words of memory.* |
| P17-/Z | P17-AA | 35V2 | |
| P17-AA | P17-/Z | 35V3 | |
| P17-BB | | | Not used for IDEEA. |
| P17-CC | | | |
| P17-DD | | | |
| P17-EE | | | |
| P17-FF | P44-/Z | NE10 | Neon driver outputs. NE10 will go from a +100 to +120 volt level to a level between 0.0V to -0.6V when computer is in a "FILL" mode. NE11 will go from a +100 to +120 volt level to a level between 0.0V to -0.6 volts when the computer is in a "VERIFY" mode. |
| P17-GG | P44-AA | NE11 | |
| P17-HH | P44-GG | F14 | Inputs to GDC M18. These inputs are to diode gates where the true state is -6 volts or open, and the false state is ground ± 1V. |
| P17-JJ | P44-HH | F15 | |
| P17-KK | P44-JJ | F16 | |
| P17-LL | P44-KK | F17 | |
| P17-MM | P44-LL | F18 | |
| P17-NN | | | Not used for IDEEA. |
| P17-PP | | | |

* The memory of M18 is divided into two portions; working and permanent, "HOT" and "COLD" respectively.

TABLE II. OPLE Logic Codes and Control Function List

| | D100 | D200 | D300 | D400 | Control Function |
|---|---|---|---|---|---|
| OPLE 0 | 0 | 0 | 0 | 0 | Not used |
| OPLE 1 | 0 | 0 | 0 | 1 | ACT Code Chemical Mode (Punch ON) |
| OPLE 2 | 0 | 0 | 1 | 0 | ACT Reader Start |
| OPLE 3 | 0 | 0 | 1 | 1 | ACT Reader Stop |
| OPLE 4 | 0 | 1 | 0 | 0 | ACT Keyboard Lock-up |
| OPLE 5 | 0 | 1 | 0 | 1 | ACU Activate |
| OPLE 6 | 0 | 1 | 1 | 0 | Digital Clock Feedback-Activate |
| OPLE 7 | 0 | 1 | 1 | 1 | Not used |
| OPLE 8 | 1 | 0 | 0 | 0 | Data Phone #1 Set-Reset |
| OPLE 9 | 1 | 0 | 0 | 1 | Data Phone #2 Set-Reset |
| OPLE 10 | 1 | 0 | 1 | 0 | ACT to M18 Activate |
| OPLE 11 | 1 | 0 | 1 | 1 | ACT Non-Code Mode (Punch OFF) |
| OPLE 12 | 1 | 1 | 0 | 0 | Punch Output |
| OPLE 13 | 1 | 1 | 0 | 1 | Not used |
| OPLE 14 | 1 | 1 | 1 | 0 | Not used |
| OPLE 15 | 1 | 1 | 1 | 1 | OPLE Reset |

TABLE III. ACT Character Set and Associated Coding

| BITS 1-7 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $b_7$ → | | | | | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| $b_6$ → | | | | | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| $b_5$ → | | | | | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| $b_4$ | $b_3$ | $b_2$ | $b_1$ | COL / ROW | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 0 | 0 | 0 | | | SPACE | $_0$0) | | Pp ⌊ | | |
| 0 | 0 | 0 | 1 | 1 | START | | | $_1$1 ⌈ | Aa α | Qq □ | | |
| 0 | 0 | 1 | 0 | 2 | | | | $_2$2° | Bb β | Rr • | | |
| 0 | 0 | 1 | 1 | 3 | | | | $_3$3: | Cc ‾ | Ss ◇ | | |
| 0 | 1 | 0 | 0 | 4 | | STOP | | $_4$4% | Dd δ | Tt i | | |
| 0 | 1 | 0 | 1 | 5 | | | "'" | $_5$5+ | Ee i | Uu \ | | |
| 0 | 1 | 1 | 0 | 6 | | | | $_6$6_ | Ff ⌋ | Vv Ↄ | | |
| 0 | 1 | 1 | 1 | 7 | | | | $_7$7' | Gg γ | Ww ● | | |
| 1 | 0 | 0 | 0 | 8 | BS | CF | | $_8$8* | Hh ⌉ | Xx ξ | | |
| 1 | 0 | 0 | 1 | 9 | TAB | | | $_9$9( | Ii / | Yy ‾ | | |
| 1 | 0 | 1 | 0 | 10 | LF | LC | | | Jj \\ | Zz - | | |
| 1 | 0 | 1 | 1 | 11 | | BR | | ï ı | Kk // | | | |
| 1 | 1 | 0 | 0 | 12 | | WR | — , ? | | Ll λ | | | |
| 1 | 1 | 0 | 1 | 13 | CR | | _ \ | | Mm μ | _/ | | |
| 1 | 1 | 1 | 0 | 14 | UC | | Δ = . | | Nn _ | | | |
| 1 | 1 | 1 | 1 | 15 | SC | | | . = | Oo ω | | | DELETE |

BS Backspace
LF Line feed
CR Carriage return
UC Upper case
SC Sub case

CF Coordinates follow
LC Lower case
BR Black ribbon
WR White ribbon

TABLE IV. Typewriter Connections and Logic Terms

| ACT Term | Interface Connection J45 | Associated M18 or Interface Term |
|---|---|---|
| Punch Coil (PC1) | J45-A | F29I |
| PC2 | J45-B | F28I |
| PC3 | J45-C | F27I |
| PC4 | J45-D | F20-I |
| PC5 | J45-E | F25I |
| PC6 | J45-F | F24I |
| PC7 | J45-G | F23I |
| PC8 | J45-H | F22I |
| Punch Clutch | J45-J | F21I |
| Select Reader Coil (SRI) | J45-K | D800 |
| SR2 | J45-L | D700 |
| SR3 | J45-M | D600 |
| SR4 | J45-N | D500 |
| SR5 | J45-P | D400 |
| SR6 | J45-R | D300 |
| SR7 | J45-S | D200 |
| SR8 | J45-T | D100 |
| Select Reader Clutch | J45-U | FB00 |
| -12V | J45-V | +38V |
| Line Advance | J45-W | OPLE 10 |
| Inhibit | J45-X | Inhibit Feedback |
| Line Advance | J45-Y | OPLE 10 |
| | J45-Z | |
| ACT Activate | J45-/A | OPLE 10 |

TABLE IV (Cont'd)

| ACT Term | Interface Connection J45 | Associated M18 or Interface Term |
|---|---|---|
| Reader Control | J45-/B | Automatic Reader Input |
| TRANSLATOR Coil (TR1) | J45-/C | D800 |
| TR2 | J45-/D | D700 |
| TR3 | J45-/E | D600 |
| TR4 | J45-/F | D500 |
| TR5 | J45-/G | D400 |
| TR6 | J45-/H | D300 |
| TR7 | J45-/I | D200 |
| TR8 | J45-/J | D100 |
| Translator Clutch | J45-/K | FB00 |
| +48V | J45-/M | +98V |
| GND | J45-/N | GND |
| Reader Control 1 | J45-/P | OPLE 2 |
| Non Code | J45-/Q | OPLE 11 |
| Code Chemical | J45-/R | OPLE 1 |
| Reader Control 2 | J45-/S | OPLE 3 |
| Reader Control 3 | J45-/T | OPLE 3 |
| Reader Input Control | J2-T (ACT Connector) | Reader Input Relay |
| Keyboard Lockup | A48-22 (ACT Card Rack) | OPLE 4 |

TABLE V. IDEEA Digital Clock Connections and Logic Terms

| | Digital Clock Term | Pin No. J19 | Associated M18 Term |
|---|---|---|---|
| Digit 1 | BCD1 | 1 | F22I |
| | BCD2 | 2 | F23I |
| | BCD4 | 3 | F24I |
| | BCD8 | 4 | F25I |
| Digit 2 | BCD10 | 5 | F26I |
| | BCD20 | 6 | F27I |
| | BCD30 | 7 | F28I |
| | BCD40 | 8 | F29I |
| | Feedback-Activate | 9 | OPLE6 |
| | Sample Data | 10 | F21I |
| | Strobe | 11 | Not used |
| | GND | 12 | GND |

TABLE VI. Bulk Storage Unit Connections

| Cable Card Pin No. | M18 Term | Interface Pin No. J42 |
|---|---|---|
| B 01 | D100 | X |
| B 02 | D200 | Y |
| B 03 | D300 | Z |
| B 04 | D400 | a |
| B 05 | D500 | b |
| B 06 | D600 | c |
| B 07 | D700 | d |
| B 08 | D800 | e |
| B 09 | AMTO | q |
| B 10 | IMTO | f |
| B 11 | FBOO | g |
| B 12 | OPL1 | h |
| B 13 | OPL2 | i |
| B 14 | TFBO | j |
| A 02 | PWR GND | p |
| B 17 | CH GND | t |
| C 01 | I1G | A |
| C 02 | I2G | B |
| C 03 | I3G | C |
| C 04 | I4G | D |
| C 05 | I5G | E |
| C 06 | I6G | F |
| C 07 | I7G | G |

TABLE VI (Cont'd)

| Cable Card Pin No. | M18 Term | Interface Pin No. J42 |
|---|---|---|
| C 08 | 18G | H |
| C 09 | TG | M |
| C 10 | FBXO | N |
| C 11 | RGO | P |
| A 01 | PWR GND | L |

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UNCLASSIFIED

Security Classification

**DOCUMENT CONTROL DATA - R & D**

*(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)*

1. ORIGINATING ACTIVITY (Corporate author)
FRANKFORD ARSENAL, Philadelphia, Pa. 19137

2a. REPORT SECURITY CLASSIFICATION
Unclassified

2b. GROUP
N/A

3. REPORT TITLE
IDEEA PROJECT FINAL REPORT - Part I. Network Development

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)
Technical research Memorandum Report

5. AUTHOR(S) (First name, middle initial, last name)
Robert J. MEENAN

6. REPORT DATE
April 1970

7a. TOTAL NO. OF PAGES
58

7b. NO. OF REFS
None

8a. CONTRACT OR GRANT NO.
AMCMS Code 5;10.21.20134

b. PROJECT NO.
DA Project 2P020401A730

c.

d.

9a. ORIGINATOR'S REPORT NUMBER(S)
FA Memorandum Report M70-18-1

9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)

10. DISTRIBUTION STATEMENT
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11. SUPPLEMENTARY NOTES

12. SPONSORING MILITARY ACTIVITY
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13. ABSTRACT

This report presents the current status of the Information Data Exchange Experimental Activities (IDEEA) Network. The Network is being developed at Frankford Arsenal for the U.S. Army Information Systems Office (CRDIS-O).

A description is given of the IDEEA console equipment, internal signal flows, and the console as a systems element. Recommendations and conclusions concerning the IDEEA console and its equipment are also presented in this report.

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